



# CBCS SCHEME

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18CS34

## Third Semester B.E. Degree Examination, Dec.2023/Jan.2024 Computer Organization

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Draw the connection between processor and memory and mention the functions of each component in the connection. (07 Marks)
- b. What is the function of an assembler directive? Give two examples of assembler directives used for the reservation of memory locations for variables state their functions. (05 Marks)
- c. With the help of suitable examples, illustrate encoding of machine instructions. (08 Marks)

OR

- 2 a. Explain how the following typical instructions can be executed with relevant steps:  
MOVE NUM1, R2  
ADD R3, NUM2 (05 Marks)
- b. Explain Big-Endian and Little-Endian method of byte addressing with an example. (07 Marks)
- c. Explain shift and rotate operations with example. (08 Marks)

### Module-2

- 3 a. Explain in brief with the help of diagram the working of daisy chain with multiple priority levels and multiple devices in each level. (10 Marks)
- b. With a block diagram, explain how the printer is interfaced to processor. (05 Marks)
- c. Briefly discuss the main phases involved in the operation of SCSI bus. (05 Marks)

OR

- 4 a. Define and explain interrupt nesting. (05 Marks)
- b. What is bus arbitration? Explain the centralized arbitration with a neat diagram. (08 Marks)
- c. Explain the tree structure of USB with split bus operation. (07 Marks)

### Module-3

- 5 a. Discuss the internal organization of a 2Mx8 asynchronous DRAM chip. (10 Marks)
- b. Briefly explain any four non-volatile memory concepts. (05 Marks)
- c. Calculate the average access time experienced by a processor if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 microseconds. (05 Marks)

OR

- 6 a. Explain the working of 16 mega byte DRAM chip configured as 1Mx16 memory chip. (10 Marks)
- b. Show with diagram the memory hierarchy with respect to speed, size and cost. (05 Marks)
- c. Define : (i) Hit rate (ii) Miss rate (iii) Miss penalty (05 Marks)

### Module-4

- 7 a. Write a note on fast adders. (05 Marks)
- b. Discuss Booth algorithm by multiplying the number -13 and +11 (08 Marks)
- c. Illustrate the steps for non-restoring division algorithm on the following data  
dividend = 1000 divisor = 11. (07 Marks)



OR

- 8 a. Write the logic diagram of 4-bit carry lookahead adder. Explain the operation. (10 Marks)  
b. Explain bit pair recording technique by multiplying the numbers +13 and -6 (06 Marks)  
c. Differentiate between restoring and non-restoring division. (04 Marks)

Module-5

- 9 a. What is pipelining? Explain the basis concept of pipeline performance with neat sketch. (08 Marks)  
b. Explain with neat diagram, microprogrammed control method for design of control unit and write the micro routine for the instruction branch  $< 0$ . (08 Marks)  
c. Differentiate between hardwired and microprogrammed control unit. (04 Marks)

OR

- 10 a. What is the purpose of control unit? With neat sketches, explain the organization of hardwired control unit in detail. (10 Marks)  
b. What is pipelining? Explain the five stage instruction pipeline with timing diagram. (10 Marks)

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