CBCS SCHEME

USN | | | | | | | | | | 18EC33

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Electronics Devices

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Outline the classficiation of material based on conductivity and energy band diagram. **(10 Marks)**

b. Classify the intrinsic and extrinisic materials, with the help of relevant diagrams. **(10 Marks)**

OR

2 a. Define mass action law. Summarize the impurity scattering and lattice scattering. **(10 Marks)**

b. Define hall effect. With the help of neat diagram, relate an expression for current density interms of conductivity and electric field. **(10 Marks)**

Module-2

3 a. Outline the qualitative description of current flow at a junction under equilibrium condition and biased conduction. **(10 Marks)**

b. Establish the operation of a PN JUNCTION diode in reverse bias condition with a neat diagram of minority carrier distributions and Fermi level variation. **(10 Marks)**

OR

4 a. Classify the Piece – wise linear approximations of junction diode under ideal condition by considering the various conditions. **(10 Marks)**

b. Describe the working of photo detectors with a relevant diagrams. **(10 Marks)**

Module-3

5 a. Summarize the charge carrier flow in a p – n – p transistor with a diagram. **(10 Marks)**

b. Illustrate the Ebers – Moll model for a PNP transistor. **(10 Marks)**

OR

6 a. Explain how BJT acts as a switch with necessary equations and diagrams. **(10 Marks)**

b. Explain the effect of base narrowing with the neat diagram and Drift in Base Region. **(10 Marks)**

Module-4

7 a. Justify "field effect transistor is a voltage controlled current device". **(10 Marks)**

b. Explain the principle of operation of n-channel enhancement mode MOSFET with a neat diagram and equations. **(10 Marks)**

OR

8 a. Illustrate the two terminal MOS structure using energy band diagram. **(10 Marks)**

b. Outline small signal equivalent circuit of JFET with neat diagram and explain the MOS structure with the aid of parallel plate capacitor. **(10 Marks)**

Module-5

9 a. Discuss the rapid thermal processing with a schematic diagram. **(10 Marks)**

b. Explain thermal oxidation process with neat diagram. **(10 Marks)**

OR

10 a. Express the integration of other circuit elements with suitable diagrams. **(10 Marks)**

b. Explain CMOS process integration. **(10 Marks)**

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