CBCS SCHEME

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17EC34

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Differentiate between :
   i) Combinational and sequential networks
   ii) Prime implicants and essential prime implicants. **(04 Marks)**

b. Simplify the given Boolean function using K-map method. Obtain minimal SOP expression $f(a, b, c, d) = \sum m(0, 1, 2, 4, 5, 7, 9, 12)$. Draw the logic diagram using only NAND gates. **(06 Marks)**

c. Construct a minimal sum for the following Boolean function using Q-M method and PI table reduction.
$f(a, b, c, d) = \sum m(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$. **(10 Marks)**

OR

2 a. Define the following terms: i) Literal ii) Maxterm iii) K-map iv) Product term. **(04 Marks)**

b. Transform the given Boolean function and express the result in decimal notation
   i) $f(a,b,c) = (a + \bar{b})(\bar{b} + c)$ into maxterm canonical formula.
   ii) $f(a, b, c) = ac + ab + bc$ into minterm canonical formula. **(06 Marks)**

c. Obtain minimal expression for the given functions using K-map
   i) Minimal product for $f(a, b, c, d) = \Pi M(0, 1, 2, 4, 5, 7, 9, 12)$
   ii) Minimal sums for $f(a, b, c) = \sum m(0, 2, 3, 4, 5, 7)$. **(10 Marks)**

Module-2

3 a. What is magnitude comparator? Design a 1-bit magnitude comparator with the help of neat logic diagram. **(06 Marks)**

b. Design binary full adder. Draw its logic diagram using 2 half adders and an OR gate. **(06 Marks)**

c. Explain the working of 4-bit look ahead carry with relevant equations and logic diagram. **(08 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$ using i) 8×1 MUX with a, b, c as select lines ii) 4×1 MUX with a, b as select lines. **(08 Marks)**

b. Realize full subtractor using 3 – to – 8 line decoder with OR gates. **(06 Marks)**

c. What is priority encoder? Design 4 – to – 2 line priority encoder with MSB having highest priority and LSB having least priority. **(06 Marks)**

Module-3

5 a. Explain the working of master-slave JK flip-flop. Draw the logic diagram using only NAND gates. **(08 Marks)**

b. Explain the operation of switch debouncer circuit using SR latch. Draw necessary waveforms. **(06 Marks)**

c. Obtain characteristic equation for SR and T flip-flops. **(06 Marks)**

OR

6 a. Explain the working of positive-edge triggered D flip-flop with the help of neat logic diagram and truth table. **(08 Marks)**

b. Explain the following timing considerations:
   i) Propagation delay in SR latch
   ii) Setup and hold time in gated D latch
   Draw necessary waveforms. **(06 Marks)**

c. Discuss the working principle of gated SR latch with logic diagram and function table. **(06 Marks)**

Module-4

7 a. Explain the operation of SISO and SIPO shift registers with an example for each. Draw the logic diagram using 4 clocked D flip-flops. **(06 Marks)**

b. Design a 3-bit binary ripple up counter using positive edge triggered T flip-flops with counting sequence and state diagram. **(06 Marks)**

c. Design Mod-6 synchronous counter using clocked SR flip-flops for the sequence 0, 2, 3, 6, 5, 1. **(08 Marks)**

OR

8 a. Explain the operation of universal shift register with a neat logic diagram and mode control table. **(06 Marks)**

b. Design a 4-bit Johnson counter using clocked D flip-flops. **(06 Marks)**

c. Design a 3-bit synchronous down counter using clocked JK flip-flop. **(08 Marks)**

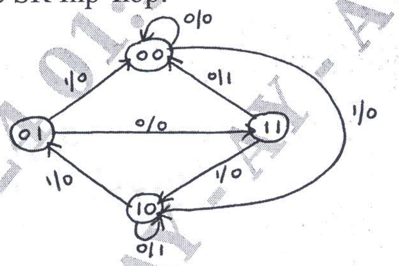
Module-5

9 a. Differentiate between Moore and Mealy model of sequential network. **(04 Marks)**

b. Construct Mealy state diagram that will detect the input sequence 10110. When input pattern is detected, Z is asserted high. **(06 Marks)**

c. Design a sequential circuit for the state diagram shown below. Consider the states as 00 – A, 01 – B, 10 – C and 11 – D. Use SR flip-flop. **(10 Marks)**

Fig.Q.9(c)



OR

10 a. Define the following terms:
   i) State variable
   ii) Excitation variable
   iii) Next state
   iv) Input variable. **(04 Marks)**

b. Design a cyclic Mod-4 synchronous binary up counter using D flip-flops. If the input variable x = 0, it remains in the same state. Otherwise moves to next state. Obtain state table, transition table, excitation table. Draw the logic diagram. **(10 Marks)**

c. Construct a Moore machine that counts the occurrences of a sequence 'abb' in any input string over {a, b}. **(06 Marks)**

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