CBCS SCHEME

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18EC62

Sixth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the architecture of ARM cortex – M3 process with the help of neat block diagram. **(10 Marks)**

b. Explain Thumb 2 technology. **(05 Marks)**

c. Explain ARM Cortex - M3 program status Register in detail. **(05 Marks)**

OR

2 a. What is stack? Explain the stack operations using PUSH and POP instructions in ARM cortex M3 with the help of neat diagram. **(06 Marks)**

b. Explain the operation modes and privilege levels in cortex M3 process with a neat transition diagram. **(08 Marks)**

c. Describe the memory map of cortex – M3 with neat diagram. **(06 Marks)**

Module-2

3 a. Explain the following instruction with example.
i) ASR ii) SXTH iii) RBIT iv) REV. **(08 Marks)**

b. Write on ALP to add two 6h-bit numbers stored in memory. **(06 Marks)**

c. Write note on barrier instruction in Cortex M3.. **(06 Marks)**

OR

4 a. Analyse the following instruction and write the contents of the register after the execution of each instruction. **(08 Marks)**
Assume $R_8 = 0 \times 00000088$ $R_9 = 0 \times 00000006$ and $R_3 = 0 \times 00001111$
i) RSB.W R_8, R_9, # 0×10
ii) ADD R_8, R_9, R_3
iii) BIC.W R_6, R_8, # 0×06
iv) ORR R_8, R_9 **(06 Marks)**

b. Explain with price of code to load multiple data into register from memory and store the same in another part of memory.

c. With a diagram, explain the organization of CMSIS and its benefits. **(06 Marks)**

Module-3

5 a. Explain the components of typical embedded system in detail. **(08 Marks)**

b. Write the difference between I2C and SPI communication interface **(06 Marks)**

c. Explain the sequence of operation of Zigbee and Wi, Fi network. **(06 Marks)**

OR

6 a. Explain sequence of operation for communicating with I2C slave device. **(08 Marks)**

b. Write the difference between RISC and CISC processors. **(06 Marks)**

c. Compare the operation of Bluetooth and Infrared. **(06 Marks)**

Module-4

7 a. What is hardware, Software co-design? Explain the fundamental issues in hardware software co-design. **(10 Marks)**

b. What is non-operational quality attribute? Explain the important non-operational any Embedded system design. **(10 Marks)**

OR

8 a. Explain high level language based embedded firmware development technique. List the advantages of this technique. **(10 Marks)**

b. What is operational quality attribute? Explain the important operational quality attributes to be considered in any embedded system design. **(10 Marks)**

Module-5

9 a. What is Kernel? What are the different functions handled by real-time Kernel? **(10 Marks)**

b. Three processes with process IDs P1, P2, P3 with estimated completion time 6, 8, 2 millisecond respectively enter the ready queue together. A new process P4 with estimated complication time 4ms enters the 'Ready' queue after 1ms. Assume all the process contains only CPU operation and no I/O operations are involved. Calculate the waiting time and Turn Around Time (TAT) for each process and the average waiting time and Turn Around Time in the SRT scheduling. **(10 Marks)**

OR

10 a. What is Inter Process Communication (IPC)? Give on overview of any two IPC mechanisms adopted by various operating systems. **(10 Marks)**

b. Three processes with process IDs P1, P2, P3 with estimated completion time 4, 6, 5 millisecond and priorities 1, 0, 3 (0-highest priority, 3-lowest priority) respectively enter the ready queue together. A new process P4 with estimated completion time 6ms and priority 2 enters the 'Ready' queue after 5ms. Calculate the waiting time and Time and Turn Around Time (TAT) for each process and the average waiting time and Turn Time (Assuming there is no I/O waiting for the processes) in priority – based scheduling algorithm. **(10 Marks)**

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