CBCS SCHEME

USN | | | | | | | | | | 18EC72

Seventh Semester B.E. Degree Examination, Dec.2023/Jan.2024
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Missing data may be suitably assumed.

Module-1

1 a. Derive an expression for drain current in linear and saturation region. **(08 Marks)**
b. Draw the CMOS inverter circuit and explain its D.C. characteristic. **(08 Marks)**
c. Implement a 2:1 MUX using transmission gate. **(04 Marks)**

OR

2 a. Explain the non ideal IV effect of MOSFET with respect to CMOS channel length modulation and mobility degradation. **(08 Marks)**
b. Explain the operation of nMOS transistor with IV characteristics. **(08 Marks)**
c. Sketch a static CMOS gate computing $y = \overline{(A + B + C)D}$. **(04 Marks)**

Module-2

3 a. Explain CMOS nWell process with necessary diagrams. **(12 Marks)**
b. Mention different types of MOSFET capacitances with necessary diagrams and equations also MOSFET. Capacitances in cut off, linear and saturation region. **(08 Marks)**

OR

4 a. Define scaling. Explain constant field scaling and constant voltage scaling and why constant voltage scaling is usually preferred over full scaling. **(07 Marks)**
b. With neat diagram, explain the Lambda based design rules for two metal layers. **(06 Marks)**
c. Draw the layout for $f = \overline{ABC}$ and estimate the cell area. **(07 Marks)**

Module-3

5 a. Develop the RC delay model to compute the delay of the logic circuit and calculate the delay of unit sized inverter driving another unit in vertex. **(06 Marks)**
b. Estimate t_{pdf} and t_{pdr} for the 3 input NAND gate shown in Fig.Q.5(b) if the output is loaded with h identical NAND gates. **(08 Marks)**

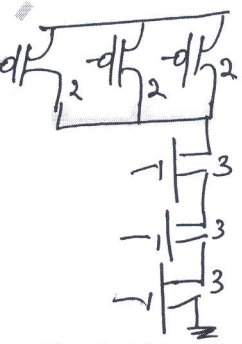


Fig.Q.5(b)

c. Explain eVSL with an example. **(06 Marks)**

OR

6 a. Explain: i) Pseudo-nMOS ii) Ganged CMOS with necessary circuit examples. **(06 Marks)**

b. If a unit transistor has R = 10KΩ and e = 0.1fF in a 65nm process, compute the delay, in picoseconds, of the inverter Fig.Q.6(b) with a fan out of h = 4. **(06 Marks)**

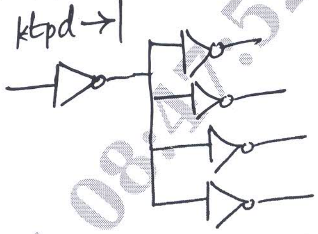


Fig.Q.6(b)

c. Explain linear delay model compare the logical effort of the following gates with the help of schematic diagrams: i) 3-input NAND gate ii) 3 input NOR gate. **(08 Marks)**

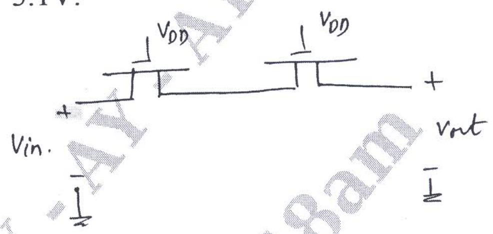
Module-4

7 a. Explain Resettable latches and flipflops using CMOS transmission gate. **(06 Marks)**

b. Explain Dynamic logic. **(06 Marks)**

c. Consider the two nFET chain in Fig.Q.7(c). The power supply is set to a value of V_{DD} = 3.3V and the nFET threshold voltage is V_{Tn} = 0.55V. Find the output voltage V_{out} at the right side of the chain for the following values: i) V_{in} = 2.9V ii) V_{in} = 3.0V iii) V_{in} = 1.4V iv) V_{in} = 3.1V. **(08 Marks)**

Fig.Q.7(c)



OR

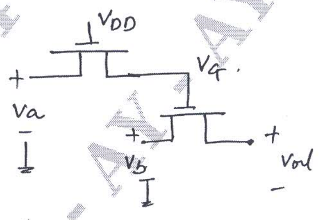
8 a. Explain pulsed latches with schematic and waveforms. **(06 Marks)**

b. The output of an nFET is used to drive the gate of another nFET as shown in Fig.Q.8(b). Assume that V_{DD} = 3.3V and V_{tn} = 0.6V. Find the output voltage V_{out} when the input voltages are at following values:

i) V_a = 3.3V and V_b = 3.3V

ii) V_a = 2.0V and V_b = 2.5V.

Fig.Q.8(b)



(08 Marks)

c. Explain Domino logic. **(06 Marks)**

Module-5

9 a. With neat schematic diagram explain the operation of Full CMOS static RAM cell. **(10 Marks)**

b. Explain the different fault models. **(10 Marks)**

OR

10 a. With neat schematic diagram explain the operation of three transistor DRAM cell. **(10 Marks)**

b. Write short notes on: i) Built in Self Test ii) Scan Design. **(10 Marks)**

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