CBCS SCHEME

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15EE34

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Analog Electronics Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the different biasing circuits of BJT, for each circuit find an expression for stability factor. Also describe how to find the Q point of the circuit. **(09 Marks)**

b. Draw the circuit of voltage divider bias. Take the circuit parameters as, $V_{CC} = 10$ V, $R_2 = 17$ KΩ, $R_1 = 83$ KΩ, $R_C = 2$ KΩ, $R_E = 0.5$ KΩ, find Q point and terminal voltages. The transistor has $\beta = 100$ and $V_{BE} = 0.7$ V. **(07 Marks)**

OR

2 a. Explain the operation of transistor as a switch with the help of neat circuit diagram and waveforms. Also enumerate the design procedure. **(08 Marks)**

b. For the following circuit, find the Q point, **(08 Marks)**

Take $V_{CC} = 10$ V, $R_C = 1$ KΩ, $R_E = 0.5$ KΩ, $\beta = 50$, $V_{BE} = 0.7$ V

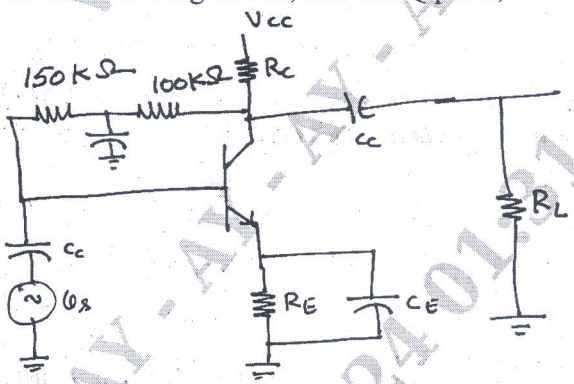

Fig. Q2 (b)

Module-2

3 a. Explain hybrid equivalent model for a transistor. Develop h-parameter model for a transistor in CE, CB and CC modes. **(08 Marks)**

b. For the common base circuit shown in Fig.Q3(b), $R_C = 10$ kΩ, $R_E = 5$ kΩ, $R_S = 1$ kΩ, $R_L = 12$ kΩ, $h_{ib} = 22\Omega$, hob = 0.49 μA/V, $h_{rb} = 2.9 \times 10^{-4}$, $h_{fb} = -0.98$, Use exact h–parameter model. Calculate A_I, Z_I, A_V and A_{VS}. **(08 Marks)**

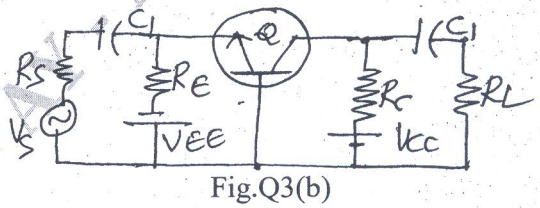

Fig.Q3(b)

OR

4 a. Explain the low frequency response by considering input RC network, output RC network. **(08 Marks)**

b. Calculate the high frequency response of amplifier circuit. Assume $R_C = 2.2k\Omega$, $R_E = 1k\Omega$, $R_1 = 68k\Omega$,, $R_2 = 22k\Omega$, $R_S = 680\Omega$, $\beta = 100$, $C_{Wi} = 6pF$, $C_{Wo} = 8pF$, $C_{ce} = 1pF$, $C_{be} = 20$ pF, $C_{bc} = 4pF$, $h_{ie} = 1.1$ kΩ, $V_{CC} = 10V$. Draw the circuit diagram. $R_L = 10k\Omega$. **(08 Marks)**

Module-3

5 a. Derive expressions for Z_i and A_i for a Darlington emitter follower circuit. **(10 Marks)**

b. Explain the need of a cascading amplifier? Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

OR

6 a. List the general characteristics of negative feedback amplifiers. **(04 Marks)**

b. Determine the voltage gain, input impedance and output impedance with feedback for voltage series feedback amplifier having $A = -100$, $R_i = 10$ kΩ, $R_o = 20$ kΩ for feedback of (i) $\beta = -0.1$ and (ii) $\beta = -0.5$. **(06 Marks)**

c. For a current series feedback amplifier, derive an expression for output impedance with feedback. **(06 Marks)**

Module-4

7 a. Draw the circuit of class-A transformed amplifier and explain its operation. Derive an expression for maximum efficiency of conversion with the help of neat waveforms. **(08 Marks)**

b. A transistor amplifier has zero signal collector current of 40 mA. When an a.c. source is connected, the dc collector current is 50 mA. The peak fundamental current in collector is 30 mA. Find second harmonic distortion and output ac power. **(08 Marks)**

OR

8 a. Draw the circuit of Wien bridge oscillator and explain its operation. Also derive an expression for frequency of oscillation. **(10 Marks)**

b. Explain with neat circuit diagram, the operation of crystal oscillator and write the expression for frequency of oscillation. **(06 Marks)**

Module-5

9 a. What are the advantages and drawback of FET Vs BJT? **(05 Marks)**

b. For the circuit shown in Fig.Q9(b), calculate V_{GSQ}, I_{DQ}, V_{DSQ} and V_D given $I_{DSS} = 10$mA and $V_p = -4V$. **(05 Marks)**

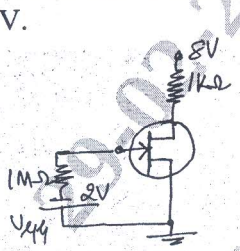

Fig.Q9(b)

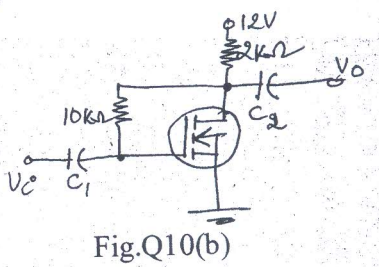

Fig.Q10(b)

c. For JFET, obtain the condition for zero current drift. **(06 Marks)**

OR

10 a. Explain construction, working and characteristics of n-channel depletion type MOSFET. **(08 Marks)**

b. For the circuit shown in Fig.Q10(b), calculate V_{GS}, I_D and V_{DS}. Given, $I_{D\ ON} = 6$mA, $V_{GS\ ON} = 8V$, $V_{GS\ TH} = 3V$. **(08 Marks)**

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