CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With basic block diagram, explain the combinational logic circuit. **(04 Marks)**

b. Reduce the following function using K-map technique and implement using basic gates

i) $f(P, Q, R, S) = \sum m(0, 1, 4, 8, 9, 10) + d(2, 11)$

ii) $f(A, B, C, D) = \pi M(0, 2, 4, 10, 11, 14, 15)$ **(12 Marks)**

OR

2 a. Simplify using the Quine-McClusky minimization technique.
$Y = f(a, b, c, d) = \sum m(0, 2, 8, 10)$ **(08 Marks)**

b. Simplify the given function using MEV technique.
$f(a, b, c, d) = \sum(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$. **(08 Marks)**

Module-2

3 a. Design a comparator to check if two N-bit numbers are equal. Configure this using cascaded stages of 1 – bit comparator. **(04 Marks)**

b. Write the compressed truth table for a 4 to 2 line priority encoder with a valid output and simplify the same using K-Map. Design the logic circuit as well. **(06 Marks)**

c. Implement the following Boolean function using a 4:1 MUX with A and B as select lines
$Y = f(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. **(06 Marks)**

OR

4 a. Write a short note on 4-bit parallel Adder. **(04 Marks)**

b. Using active high output 3:8 line decoder, implement the following functions
$f_1(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 11, 15)$
$f_2(A, B, C, D) = \sum m(1, 3, 4, 11, 13, 14)$ **(06 Marks)**

c. Design an 8:1 MUX Tree using only 2:1 multiplexers. **(06 Marks)**

Module-3

5 a. Explain the operation of Master-Slave JK flip-flop with logic diagram, truth table, symbol and timing diagram. **(08 Marks)**

b. Distinguish between sequential circuits and combinational circuits. **(04 Marks)**

c. Explain the operation of basic bistable element, using two-inverter configuration. **(04 Marks)**

OR

6 a. Derive characteristics equations for SR flip-flop and JK flip-flop, represent truth table and K-maps. **(04 Marks)**

b. Explain the operation of 4-bit ring counter and twisted ring counter. **(06 Marks)**

c. Design synchronous MOD6 counter using clocked 'D' flip flops for the sequence $0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 5 \rightarrow 1$, again, 0.... represent application table, excitation table and logic diagram. **(06 Marks)**

Module-4

7 a. Distinguish between Moore and Mealy model with necessary block diagrams. **(08 Marks)**

b. Give output function, transition table and state diagram by analyzing the sequential circuit shown in Fig. Q7(b). **(08 Marks)**

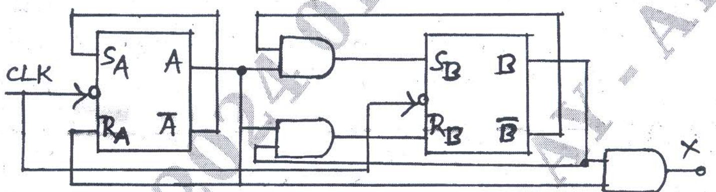

Fig. Q7(b)

OR

8 a. Write the basic recommended steps for the design of a clocked synchronous sequential circuit. **(06 Marks)**

b. Design a synchronous counter using J-K flip flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 Use state diagram and state table. **(10 Marks)**

Module-5

9 a. Mention styles/types of HDL description. Explain behavioral type with half adder example in both VHDL and verilog. **(08 Marks)**

b. Compare VHDL and verilog. **(04 Marks)**

c. Explain verilog data types. **(04 Marks)**

OR

10 a. Tabulate Rotate operators used in HDL with example operand A = 1110. **(08 Marks)**

b. Draw the block diagram of 3-bit carry look ahead adder. Write verilog code for the same. **(08 Marks)**

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