CBCS SCHEME

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15EE46

Fourth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Operational Amplifiers and Linear ICs

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. What is an op-amp? Explain the operation of block diagram representation of a typical op-amp. **(05 Marks)**

b. Briefly explain the difference between the DC and AC amplifiers. **(03 Marks)**

c. With a neat circuit diagram, explain the operation of the non-inverting amplifier with feedback. Derive an expression for a closed loop voltage gain (A_F) and input resistance with feedback (R_{iF}). **(08 Marks)**

OR

2 a. Explain the following electrical parameter :
i) Input offset voltage
ii) CMRR
iii) Slew rate. **(06 Marks)**

b. What are the characteristics of an ideal op-amp? **(04 Marks)**

c. Use a 741 op-amp, design a summing amplifier to add three DC input voltages. The output voltage (V_0) of this circuit must be equal to two times the negative sum of the input. **(06 Marks)**

Module-2

3 a. Draw the circuit diagram derive expression for the voltage gain and phase angle of first order low-pass Butterworth filter. **(04 Marks)**

b. Design a second order high-pass filter circuit to have cutoff frequency of 1KHz, Shows the nature of frequency response. **(06 Marks)**

c. Using LM 317 IC regulator, design an adjustable voltage regulator to satisfy the following specification output voltage V_0 = 5V to 12V, output current I_0 = 1.0A. (V_{ref} = 1.25V, I_{adj} = 100μA). **(06 Marks)**

OR

4 a. Sketch the circuit of a voltage follower regulator. Explain the circuit operation. **(04 Marks)**

b. Explain the following performance parameter of voltage regulator :
i) Line regulation
ii) Load regulation
iii) Ripple rejection. **(06 Marks)**

c. Using a 741 op-amp, design a single stage band filter to have a voltage gain of 1 and a pass-band from 300Hz to 30 KHz. **(06 Marks)**

Module-3

5 a. With a neat circuit diagram and relevant waveforms, explain the operation of a triangular /rectangular waveform generator which has frequency and duty cycle controls. **(10 Marks)**

b. Design a non-inverting Schmitt trigger circuit to have UTP = +3V and LTP = –5V. Use a 741 ICs with supply V_{CC} = ±15V, choose I_{Bmax} = 500nA. **(06 Marks)**

OR

6 a. Draw the circuits of an op-amp inverting zero-crossing detector and a voltage level detector. Explain operation of each circuits. **(04 Marks)**

b. Design a RC phase shift oscillator to have an output frequency of 3.5KHz. Use a 741 op-amp with a voltage supply of ±12V. **(06 Marks)**

c. With a neat circuit diagram and waveforms, explain the operation of a Wein bridge oscillator. **(06 Marks)**

Module-4

7 a. Sketch the circuit of a non-saturating half wave precision rectifier and explain the operation of the circuit. Draw the input – output waveform. **(04 Marks)**

b. Draw a neat circuit diagram, explain the working operation of R-2R ladder DAC. Shows the graph of output versus inputs. **(08 Marks)**

c. With a neat circuit diagram, explain the working of voltage follower type peak detector. **(04 Marks)**

OR

8 a. Design a adjustable peak clipping circuit to clip at approximately ±(3V to 5V). The circuit is to have unity voltage gain before clipping. **(08 Marks)**

b. Briefly describe the operation of successive approximation analog to digital converter with neat block diagram. **(08 Marks)**

Module-5

9 a. What is Phase Locked Loop (PLLs)? Explain the working of the building blocks of PLL. **(08 Marks)**

b. With a neat circuit, explain the functional diagram of IC 555 timer. **(08 Marks)**

OR

10 a. With a neat sketch, explain the operation of a monostable multivibrator using IC555 timer and also draw the input and output waveforms. **(06 Marks)**

b. Using IC555 timer, design an astable multivibrator having an output frequency of 10KHz with a duty cycle of 25%. **(06 Marks)**

c. Explain the concepts of a low pass filter and VCO in Phase Locked Loop. **(04 Marks)**

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