CBCS SCHEME

USN | | | | | | | | | | |

15MT36

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Computer Organization

Time: 3 hrs. Max. Marks : 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the basic operational concepts between the processor and memory. **(08 Marks)**

b. How to measure the performance of the computer using performance equation? **(08 Marks)**

OR

2 a. Explain the following instruction with example :
i) MOVE LOC, R1 ii) ADD A, B, C iii) STORE R_i, A
iv) LOAD A, R_6 v) SUBTRACT$(R1)_1$+ R5 **(10 Marks)**

b. Explain BIG-ENDIAN and LITTLE – ENDIAN methods with example. **(06 Marks)**

Module-2

3 a. Explain with example the following addressing modes:
i) Indirect mode ii) Indexing mode iii) Absolute mode. **(08 Marks)**

b. Explain shift and rotate instruction with example. **(08 Marks)**

OR

4 a. Explain the format of IEEE standard for floating point number. Also explain how normalization in IEEE is carried out. **(08 Marks)**

b. Discuss the following in case of subroutine:
i) Subroutine nesting ii) Parameter passing. **(08 Marks)**

Module-3

5 a. Define memory mapped I/O and I/O mapped I/O with example. **(04 Marks)**

b. Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line. **(04 Marks)**

c. Describe DMA concept in brief. **(08 Marks)**

OR

6 a. Define bus arbitration. Explain in detail any one approach of bus arbitration. **(08 Marks)**

b. Discuss briefly the protocols of USB. **(08 Marks)**

Module-4

7 a. Discuss different mapping functions in case of cache. **(08 Marks)**

b. Explain SDRAM with the help of neat block diagram. **(08 Marks)**

OR

8 a. Discuss internal organization of 2M × 8 dynamic memory chips. **(05 Marks)**

b. Explain the memory hierarchy with neat diagram. **(05 Marks)**

c. Briefly discuss virtual memory organization. **(06 Marks)**

Module-5

9 a. Explain with neat diagram single bus organization of the data path inside processor. **(08 Marks)**

b. Analyze of explain the concepts of :
i) Fetching a word from memory
ii) Storing a word in memory. **(08 Marks)**

OR

10 a. Explain the block diagram of the basic organization of a microprogrammed control unit. **(08 Marks)**

b. Explain microinstruction sequencing with next address field. **(08 Marks)**

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