CBCS SCHEME

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18MT36

# Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
## Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

**Note:** ***Answer any FIVE full questions, choosing ONE full question from each module.***



### Module-1

1 a. Discuss the block diagram of basic functional unit of computer. **(06 Marks)**

b. Explain the basic instruction types with example. **(06 Marks)**

c. How to measure the performance of the computer? Explain. **(08 Marks)**

**OR**

2 a. With neat diagram, explain the byte addressability Big-endian and Little-endian assignments. **(10 Marks)**

b. Explain with a neat diagram, the correction between processor and computer memory and also typical operating steps for executing an instruction. **(10 Marks)**

### Module-2

3 a. What is subroutine? Explain subroutine linkage method with an example. **(10 Marks)**

b. Explain the following :

i) Logical shaft left
ii) Logical shift right
iii) Rotate left
iv) Rotate right
v) Arithmetic shift right. **(10 Marks)**

**OR**

4 a. Explain the principle of operation of stack with suitable instruction and diagram. **(10 Marks)**

b. Write a short note on the following :

i) Assembly language
ii) Assembler directive. **(10 Marks)**

### Module-3

5 a. Explain the concept of DMA controller with suitable diagram along with register and parameters. **(10 Marks)**

b. What is I/O interface? With a neat diagram, explain hardware arrangement. **(10 Marks)**

**OR**

6 a. With a neat diagram of timing, explain how input transfer happens on synchronous bus. **(10 Marks)**

b. What is interrupt nesting? Explain with a neat diagram the implementation of interrupt priority using individual interrupt request and acknowledge lines. **(10 Marks)**

### Module-4

7 a. Explain the asynchronous DRAM operation with a neat block diagram. **(10 Marks)**

b. Draw the organization of 16 × 8 memory chip and explain it working. **(08 Marks)**

c. What is virtual memory technique? **(02 Marks)**

**OR**

8 a. What is meant by cache? With a neat block diagram, explain the direct and set associative mapping between cache and main memory. **(10 Marks)**

b. Define ROM. List and explain various types of ROMs. **(06 Marks)**

c. Explain read and write operation in static memory. **(04 Marks)**

## Module-5

9 a. Define memory Read operation. Mention the steps for memory read operation. **(10 Marks)**

b. Describe micro-programmed control unit organization with a neat diagram. **(10 Marks)**

**OR**

10 a. Explain multiple bus organization of the data path with a neat diagram. **(10 Marks)**

b. With a neat diagram, explain hardwired control unit shows the generation Zin and End control signal. **(10 Marks)**

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