CBCS SCHEME

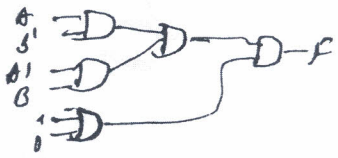
USN | | | | | | | | | | |

BCS302

Third Semester B.E./B.Tech. Degree Supplementary Examination
June/July 2024
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. *Answer any FIVE full questions, choosing ONE full question from each module.*
2. *M : Marks , L: Bloom's level , C: Course outcomes.*

		Module – 1	M	L	C
Q.1	a.	Simplify the Boolean function i) $F(x, y, z) = \Sigma(2, 3, 4, 5)$ ii) $F(x, y, z) = \Sigma(3, 4, 6, 7)$	10	L3	CO1
	b.	Obtain a minimum product of sum with a Karnaugh Map $F(w, x, y, z) = x'z' + wyz + w'y'z' + x'y$	10	L3	CO1
		OR			
Q.2	a.	Define multiplexer. Explain 2 to 1 line multiplexer.	10	L2	CO1
	b.	Write the verilog code and time diagram for the given circuit with propagation delay where the AND, OR gate has a delay of 30ns and 10ns.  Fig Q2(b)	5	L2	CO1
	c.	Explain implementation of full adder with logic diagram.	5	L3	CO1
		Module – 2			
Q.3	a.	Explain with neat diagram and 4 input priority encodes.	10	L2	CO2
	b.	Explain 2 : 4 time decoder with help of logic diagram and truth table.	10	L2	CO2
		OR			
Q.4	a.	Define Latch. Explain S-R flip flop based on NOR Gate with neat diagram.	10	L2	CO2
	b.	Explain clocked D flip flop with neat diagram.	10	L2	CO2
		Module – 3			
Q.5	a.	With neat diagram, explain the basic operational concepts of computers.	10	L2	CO3
	b.	Write a program to evaluate arithmetic statement Y = (A + B) * (C + D) using 3 address, 2 address, one address and zero address instruction.	10	L3	CO3
		OR			
Q.6	a.	Describe the concept of Blanch instruction with example.	10	L2	CO3
	b.	Explain 5 addressing modes with example.	10	L2	CO3

		Module – 4			
Q.7	**a.**	Explain the I/O interfacing and I/O device with computers.	**10**	**L2**	**CO4**
	b.	What is Bus Arbitration? Explain types of bus arbitration.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	What is cache memory? Explain the different type of cache mapping function.	**10**	**L2**	**CO4**
	b.	Explain basic concepts involved for memory structures of computers.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Explain with neat diagram of single bus organization.	**10**	**L2**	**CO5**
	b.	Explain complete execution steps for instruction ADD (R3), R1.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain execution of complete instruction carry out.	**10**	**L2**	**CO5**
	b.	What is pipeline? Explain with example of pipeline performance.	**10**	**L2**	**CO5**

* * * * *