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BCS402

Fourth Semester B.E./B.Tech. Degree Supplementary Examination, June/July 2024
Microcontrollers

Time: 3 hrs.

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	List and explain 4 major design rules in RISC design philosophy.	10	L2	CO1
	b.	With a neat diagram explain ARM based embedded device, a microcontroller.	10	L2	CO1
		OR			
Q.2	a.	Explain in detail ARM Design Philosophy.	10	L2	CO1
	b.	Explain in detail software abstraction layers executing on hardware (embedded system software).	10	L2	CO1
		Module – 2			
Q.3	a.	Explain arithmetic and logical data processing instructions with syntax, examples and code snippet for each.	10	L3	CO2
	b.	Explain four steps of stack implementation in ARM with examples for each.	10	L2	CO2
		OR			
Q.4	a.	Write note on : i) Coprocessor Instructions ii) Software Interrupt instructions	10	L2	CO2
	b.	Develop ARM ALP to find largest number in an array of 32 bit numbers. Program should be neatly commented.	10	L3	CO2
		Module – 3			
Q.5	a.	Discuss with C function and target ARM assembly code how optimization can be done with respect to data types.	10	L2	CO3
	b.	Explain optimizations with respect to C loop structures considering fixed number of iterations, variable number of iterations and loop unrolling. Explain with examples for each.	10	L2	CO3
		OR			
Q.6	a.	Discuss and analyze optimization with respect to pointer aliasing, effects of pointer aliasing with simple C code / function.	10	L3	CO3
	b.	Analyze and explain the way structure arrangement to be done in order to access the structure members efficiently.	10	L3	CO3
		Module – 4			
Q.7	a.	Discuss the following : i) Interrupt latency ii) Types of interrupts available on ARM processor.	10	L2	CO4
	b.	Write short code snippet to enable and disable interrupts. Explain in detail.	10	L3	CO4
		OR			
Q.8	a.	What is firmware? Explain firmware execution flow and bootloader.	10	L2	CO4
	b.	Explain / Discuss Sandstone execution flow in detail.	10	L2	CO4
		Module – 5			
Q.9	a.	Discuss basic architecture of a cache memory with a neat diagram.	10	L2	CO5
	b.	Explain in detail memory hierarchy and cache memory.	10	L2	CO5
		OR			
Q.10	a.	Discuss Cache policy in detail.	10	L2	CO5