CBCS SCHEME

USN | | | | | | | | | | |

18EE35

Third Semester B.E. Degree Examination, June/July 2024
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Using the K-map determine the minimal sum of the Boolean function f(A, B, C, D) = ∑m (0, 2, 3, 5, 7, 8, 9) + d.c ∑m (10, 11, 12, 13, 14, 15). **(06 Marks)**

b. Convert the following expression to its canonical form
i) x = A + BC + ABC
ii) f = A(B + C) (A + B + C) **(04 Marks)**

c. Using Quine Mc Cluskey method obtain a minimal SOP expression for f(A, B, C, D) = ∑m (0, 1, 4, 5, 8, 9, 10, 11, 13, 15). **(10 Marks)**

OR

2 a. Using the K-map determine the minimal sum of the Boolean function f(A, B, C, D, E) = ∑m (0, 4, 5, 8, 12, 13, 16, 20, 21, 24, 28, 29). **(07 Marks)**

b. What is a K-map? Which is the code used to number cells/boxes, row and column heading of a K-map. Write a neat numbered 3-variable K-map. **(06 Marks)**

c. Using K-map, evaluate the minimal POS expression of f(w, x, y, z) = πM (0, 2, 3, 8, 12, 14) . d.c πM (1, 4, 5, 11, 15). **(07 Marks)**

Module-2

3 a. With a neat diagram, explain the operation of a carry look ahead adder circuit. **(08 Marks)**

b. Implement full adder using TWO 4:1 MUX. **(05 Marks)**

c. Design two 2-bit magnitude comparator and implement the circuit with only NAND gates. **(07 Marks)**

OR

4 a. Explain the operation of a decimal to BCD priority encoder. **(08 Marks)**

b. Implement full subtractor with two half subtractor with external circuit. **(05 Marks)**

c. Implement 16:1 MUX using five numbers of 4:1 MUX. **(07 Marks)**

Module-3

5 a. Explain the working of master slave (M-S) J-K flip flop with functional table and timing diagram also explain how race around condition is eliminated. **(10 Marks)**

b. Obtain characteristic equation of J-K flip flop. **(04 Marks)**

c. How an S-R flip flop is converted to J-K flip flop? **(06 Marks)**

OR

6 a. What is a flip flop? Explain the types of flip flops any three. **(06 Marks)**

b. With the neat diagram, explain positive edge triggered J-K flip-flop. **(08 Marks)**

c. Explain the gated latch in a flip-flop. Obtain characteristic equation of S-R flip-flop. **(06 Marks)**

Module-4

7 a. What are registers? Explain the four modes of operation of a shift register with suitable logic diagram. **(08 Marks)**

b. Explain working of 3-bit binary ripple counter with suitable logic and timing diagram. **(06 Marks)**

c. With logic diagram and truth table explain mod-4 ring counter. **(06 Marks)**

OR

8 a. Design mod-6 synchronous counter using S-R flip flop. Consider the count as $0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 5 \rightarrow 1 \rightarrow 0$ **(10 Marks)**

b. Design a synchronous counter to count from 0000 to 1001 using J-K flip-flop using minimal combination gating. **(10 Marks)**

Module-5

9 a. With the neat block diagram, explain the Mealy and Moore clocked synchronous sequential circuits. **(10 Marks)**

b. Analyze the following synchronous sequential circuit to obtain input equations, excitation table and state diagram as shown in Fig.Q.9(b). **(10 Marks)**

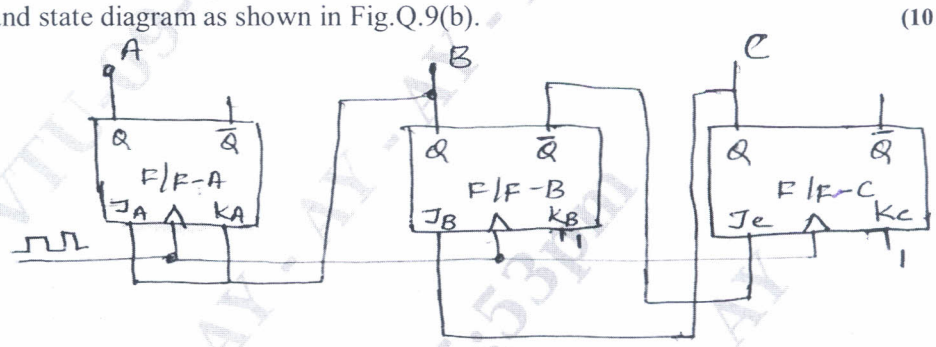

Fig.Q.9(b)

OR

10 a. Explain the following:
Read Only Memory (ROM)
Read/Write Memory (R/W M)
Flash Memory. **(12 Marks)**

b. Using the 3:8 decoder of 74138, design the ROM for given truth table, explain its operation

I/P's			O/P'S			
A_3	A_2	A_1	D_4	D_3	D_2	D_1
0	0	0	0	0	0	1
0	0	1	0	1	0	1
0	1	0	1	0	0	0
0	1	1	1	1	0	1
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	1	0	1	0
1	1	1	1	0	0	1

(08 Marks)

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