CBCS SCHEME

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BEE306A

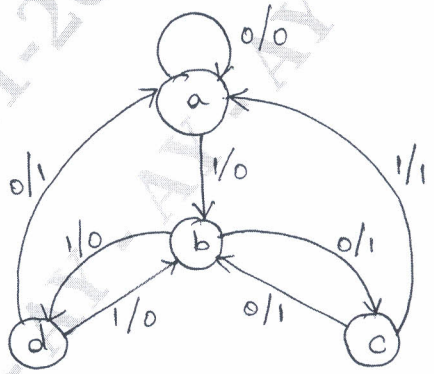
Third Semester B.E./B.Tech. Degree Supplementary Examination, June/July 2024

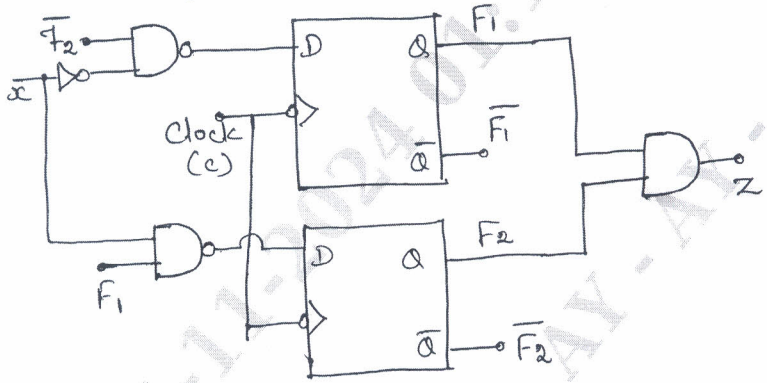
Digital Logic Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a basic block diagram, explain the combinational logic circuit. List the various steps in designing the combinational logic circuit.	6	L1	CO1
	b.	Convert the given Boolean function in both canonical maxterm and minterm forms in decimal notation. i) $f = \bar{x}y + yz$ ii) $f = (\bar{a} + b)(b + \bar{c})$	8	L2	CO1
	c.	Simplify the given function using K-map and write the simplified SOP and POS expression. $y = f(a, b, c, d) = \pi M (0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$	6	L2	CO1
		OR			
Q.2	a.	Using K-map method, obtain minimal SOP expression and implement the function using NAND gates. $X = f(a, b, c, d, e) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30)$.	8	L3	CO1
	b.	Obtain all the prime implicants of the given Boolean function using Quine-Mcclurkey method and verify the result using K-map technique $f(a, b, c, d) = \sum m(0, 2, 3, 5, 8, 10, 11)$.	12	L3	CO1
		Module – 2			
Q.3	a.	Design a combinational logic circuit that will convert BCD to excess 3 code converter. Construct truth table and simplify each output equation using K-maps.	8	L3	CO2
	b.	Construct the truth table and design a binary full adder using NAND gates.	7	L2	CO2
	c.	Realize 4:16 decoder using 3:8 decoder and write its truth table.	5	L2	CO2
		OR			
Q.4	a.	Design two bit magnitude comparator and draw its logic diagram.	10	L3	CO2
	b.	Implement the given function using 4:1 MUX. Use ab as select lines $y = f(p, q, r, s) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$.	5	L4	CO2
	c.	Draw the circuit and explain the operation of look ahead carry adder.	5	L2	CO2

		Module – 3			
Q.5	**a.**	Explain the working of Master Slave JK flip flop. Draw its logic diagram, function table, symbol and timing diagram.	**12**	**L2**	**CO3**
	b.	Explain the operation of SR latch as switch debouncer. Draw its timing diagram.	**8**	**L2**	**CO3**
		OR			
Q.6	**a.**	Obtain the characteristics equation of JK and D flip flop.	**5**	**L2**	**CO3**
	b.	Differentiate sequential logic circuit and combinational circuit.	**5**	**L2**	**CO3**
	c.	With a neat circuit diagram, explain the working of positive edge triggered D flip flop. Write its function table and symbol.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With a neat logic diagram, explain the operation of 4 bit universal shift register using D-flipflop. Write the mode control table of universal shift register.	**10**	**L2**	**CO4**
	b.	Design a synchronous counter for 5421 code sequencer using positive edge triggered D flip flop with minimal combinational circuits.	**10**	**L4**	**CO4**
		OR			
Q.8	**a.**	Design 4 bit binary ripple up counter using negative edge triggered JK flip flops. Explain its operation, write its truth table and draw its timing diagram.	**10**	**L4**	**CO4**
	b.	Design synchronous Mod-6 counter using clocked JK flip flop.	**10**	**L4**	**CO4**
		Module – 5			
Q.9	**a.**	With relevant block diagram, explain Moore and Mealy model.	**8**	**L2**	**CO5**
	b.	Construct a sequential logic circuit with single input x and single output Z by obtaining the state and excitation table for the given state diagram shown in Fig.Q.9(b) using JK flip flop.  Fig.Q.9(b)	**12**	**L3**	**CO5**

		OR			
Q.10	**a.**	For the given logic diagram shown in Fig.Q.10(a), derive the excitations output equations, write the next state equations, construct transition table and draw its state diagram.  Fig.Q.10(a)	**12**	**L3**	**CO5**
	b.	Write short note on the following with suitable diagram: i) ROM ii) PROM iii) Flash memory.	**8**	**L2**	**CO6**

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