

CBCS SCHEME

18EE34



Third Semester B.E. Degree Examination, June/July 2024

Analog Electronic Circuits

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat circuit diagram and waveforms explain simple positive series clipper. Also draw the transfer characteristics. (10 Marks)
- b. What is biasing? What are the requirements of biasing circuits? With neat circuit diagram explain Emitter stabilized bias circuit. (10 Marks)

OR

- 2 a. The circuit shown in Fig.Q2(a), for $R_B = 300 \text{ k}\Omega$ and $R_C = 150 \text{ k}\Omega$, calculate I_B , I_C and V_{CE} and determine region of operation.

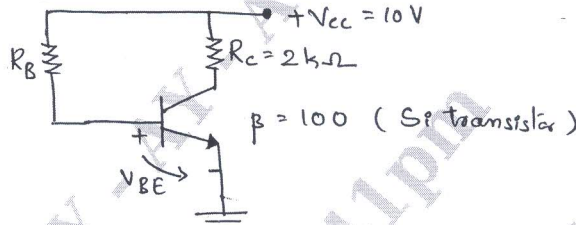


Fig.Q2(a)

(10 Marks)

- b. Derive stability factors for fixed bias circuit:
 - i) $S_{(I_{CO})}$ ii) $S_{(V_{BE})}$ iii) $S_{(\beta)}$ (06 Marks)
- c. Draw and explain switching characteristics of transistor. (04 Marks)

Module-2

- 3 a. Derive expressions for A_v , Z_i and Z_o of voltage divider bias circuit using hybrid model. (10 Marks)
- b. A common collector circuit shown in Fig.Q3(b) has following components :
 $R_1 = 27\text{k}\Omega$, $R_2 = 27\text{k}\Omega$, $R_E = 5.6\text{k}\Omega$, $R_L = 47\text{k}\Omega$, $R_S = 600\Omega$. The transistor parameters are $h_{ie} = 1 \text{ k}\Omega$, $h_{fe} = 85$ and $h_{oe} = 2 \mu\text{A/V}$. Calculate (i) A_i (ii) R_i (iii) A_v (iv) R_o

(v) $A_{vs} = \frac{V_o}{V_s}$ (vi) $A_i = \frac{I_o}{I_s}$

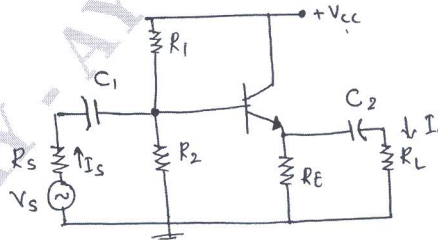


Fig.Q3(b)

(10 Marks)

OR

- 4 a. State and prove Miller's theorem. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

- b. Fig.Q4(b) shows a single stage CE amplifier with unbypassed emitter resistance. Find
 (i) A_i (ii) R_i (iii) A_v (iv) A_{vs} (v) A_i

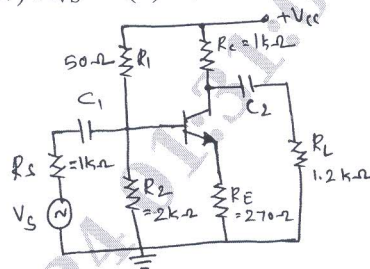


Fig.Q4(b)

(10 Marks)

Module-3

- 5 a. Explain need for cascading of amplifiers. (04 Marks)
 b. Explain with a neat block diagram Two stage cascaded amplifier. (06 Marks)
 c. Derive A_i , Z_0 and A_v for Darlington Emitter follower. (10 Marks)

OR

- 6 a. Explain with neat block diagram concept of feedback amplifier. (10 Marks)
 b. Derive the expression for output resistance for a voltage series feedback amplifier and voltage shunt feedback amplifier (10 Marks)

Module-4

- 7 a. Explain with neat circuit diagram transformer coupled class A amplifier. Derive equation for maximum efficiency. (10 Marks)
 b. Explain classification of Power amplifiers. (10 Marks)

OR

- 8 a. Explain with neat circuit diagram R-C phase shift oscillator. (10 Marks)
 b. In a Wein bridge oscillator $R_1 = R_2 = 100k\Omega$ and ganged variable capacitor has a range from 50 pF to 500 pF. Find the range of frequency of the oscillations possible. If the frequency derived is 50 kHz more than the maximum frequency calculated above, find the value of resistance to be connected in parallel with 100 kΩ. (10 Marks)

Module-5

- 9 a. Explain construction of n-channel JFET and also explain the working principle. (10 Marks)
 b. The p-channel FET has a $|I_{DSS}| = -12 \text{ mA}$; $|V_p| = 5V$, V_{GS} is 5.32V. Calculate I_D , g_m and g_{m0} . (10 Marks)

OR

- 10 a. With neat diagram explain constructional details of P-channel depletion type MOSFET and also explain its working. (10 Marks)
 b. For the circuit shown in Fig.Q10(b), calculate (i) I_D (ii) V_{GS} (iii) V_G (iv) V_{DS} (v) V_s

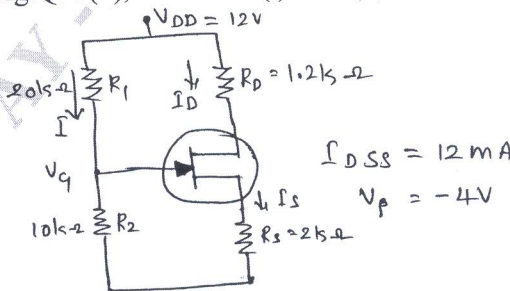


Fig.Q10(b)

** 2 of 2 **

(10 Marks)