



## Third Semester B.E. Degree Examination, June/July 2024 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Explain the operation of a computer with neat block diagram. (10 Marks)
- b. Explain system software functions in detail. (05 Marks)
- c. Explain bus structures. (05 Marks)

OR

- 2 a. Define byte addressability, Big-endian and Little-endian assignment (06 Marks)
- b. Explain following registers : (06 Marks)
- i) PC    ii) IR    iii) MAR.
- c. Explain basic performance equation. (08 Marks)

### Module-2

- 3 a. List and explain the generic addressing modes with assembler syntax and addressing function. (10 Marks)
- b. What are assembler directives? Explain any five assembler directives. (10 Marks)

OR

- 4 a. Explain stack concepts with diagram. (08 Marks)
- b. Explain shift and rotate operations with examples. (06 Marks)
- c. List the steps involved in 'CALL' and 'RETURN' instructions. (06 Marks)

### Module-3

- 5 a. Explain memory mapped I/O access. (10 Marks)
- b. What is an interrupt? With an example explain the concept of interrupt. (10 Marks)

OR

- 6 a. Explain Daisy chain method used for handling simultaneous interrupt request. (08 Marks)
- b. Explain the use of DMA controller in computer system. (06 Marks)
- c. Explain the concept of vectored interrupt. (06 Marks)

### Module-4

- 7 a. Explain the internal organization of  $2M \times 8$  dynamic memory chip. (10 Marks)
- b. Explain virtual memory organization. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 8 a. Explain secondary storage device. (08 Marks)  
b. Explain cache memory and its relevant terms. (06 Marks)  
c. Explain different types of non volatile memory. (06 Marks)

Module-5

- 9 a. Discuss the single bus organization of data path inside a processor. (10 Marks)  
b. Draw and explain multiple bus organization of CPU. (10 Marks)

OR

- 10 a. Explain block diagram of a complete processor. (08 Marks)  
b. Explain micro programmed control concept. (06 Marks)  
c. Discuss the organization of hardwired controlled unit. (06 Marks)

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