CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Supplementary Examination, June/July 2024

Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain with a neat block diagram, the steps involved in realizing logic circuit from a problem statement.	06	L1	CO1
	b.	Identify the prime implicants and essential prime implicants of the following functions using Karnaugh map. i) $f(a, b, c, d) = \Sigma m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$ ii) $f(a, b, c, d) = \prod M(0, 2, 3, 8, 9, 10, 12, 14)$	10	L2	CO1
	c.	Express the equation in proper canonical form: $G = f(w, x, y, z) = w'x + yz'$	04	L2	CO1
		OR			
Q.2	a.	Simplify the following equation $S = f(w, x, y, z) = \Sigma(1, 3, 13, 15) + \Sigma d(8, 9, 10, 11)$ using Quine – McClusky technique.	12	L2	CO1
	b.	An electric motor powering a conveyor used to move material is to be turned on when one of two operators is in position. If material is present to be moved and if the protective interlock switch is not open input and output variables are to expressed in binary, that is, if operator 1 is in position and the associated variable is a logical 0. The motor is running (on) if its output control variable is a '1' and the motor is off if the output variable is 0. write the truth table for the control problem and write the switching equation for the output that turns the motor ON.	08	L3	CO1
		Module – 2			
Q.3	a.	Explain the need for look ahead carry adders in reduction of propagation of delay by considering 4-bit parallel look ahead carry adder and deriving relevant equations at each stage.	12	L2	CO2
	b.	What are Decoders? Implement the following functions using a 3 to 8 line decoder: i) $f_1(a, b, c) = \Sigma m(0, 4, 6, 7)$ ii) $f_2(a, b, c) = \prod M(1, 4, 5)$	08	L2	CO2
		OR			
Q.4	a.	With a neat block diagram, explain decimal adders. Write a truth table to show decimal SUM, Binary SUM and BCD SUMS. Also generate the correction function from the truth table.	10	L2	CO2
	b.	Define encoders. Design a 8 to 3 line priority encoder with a neat truth table and write Boolean expressions for the outputs.	10	L4	CO2
		Module – 3			
Q.5	a.	Explain the operation of Master-Slave SR Flip-Flop with relevant waveforms.	10	L3	CO3
	b.	Derive the characteristic equations for SR, JK, D and T flip-flops from their respective functional tables.	10	L3	CO3

		OR			
Q.6	**a.**	What are registers? Illustrate the four possible ways through which registers transfer information.	**10**	**L2**	**CO3**
	b.	Design a synchronous mod-6 counter using clocked JK flip flops.	**10**	**L4**	**CO3**
		Module – 4			
Q.7	**a.**	Explain the structure of a verilog module and list out the various operator used in verilog coding with examples.	**10**	**L4**	**CO4**
	b.	Write a verilog code for a 2:1 multiplexer with necessary logic diagram and simulation waveforms.	**10**	**L3**	**CO4**
		OR			
Q.8	**a.**	Explain the different types of descriptions used in verilog coding.	**10**	**L3**	**CO4**
	b.	Write a verilog code using dataflow description for a half adder with necessary waveforms and truth table.	**06**	**L3**	**CO4**
	c.	Write a verilog code for the Boolean expressions given below: $Y_1 = ab'c + ab + (a \oplus b)$ $Y_2 = (wx) + (w'y) + w\ x\ y$	**04**	**L3**	**CO4**
		Module – 5			
Q.9	**a.**	With necessary flow chart explain D-latch along with a verilog code and simulation waveform.	**10**	**L3**	**CO5**
	b.	With necessary logic diagram, explain behavioural description for a 3-bit Binary counter using case statements in verilog code.	**10**	**L3**	**CO5**
		OR			
Q.10	**a.**	Differentiate case X and case Z statements in verilog and write a verilog code for a 4-bit priority encoder using case X statement.	**10**	**L3**	**CO5**
	b.	With necessary flow chart explain Booth multiplication algorithm and write a verilog code for the same.	**10**	**L3**	**CO5**

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