CBCS SCHEME

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BEC306C

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat diagram, describe the functional units of a computer. Give examples for I/O.	10	L2	CO1
	b.	Write assembly language program for X = (A * B) + (C * D) using one address, two address, and three address instructions formats.	06	L3	CO1
	c.	Explain the Bus structures.	04	L2	CO1
		OR			
Q.2	a.	With a neat diagram, discuss the operational concepts in a computer highlighting the role of PC, MAR, MDR, IR.	10	L2	CO1
	b.	Discuss IEEE standard for single precision and double precision floating point numbers with standard notations.	06	L3	CO1
	c.	Distinguish between Big-endian and Little-endian memory assignment. With a neat sketch, show how the value 26789435 is stored using these methods.	04	L3	CO1
		Module – 2			
Q.3	a.	Define addressing mode. Explain any five addressing mode with syntax and examples.	10	L2	CO2
	b.	What is subroutine? With a pseudocode or program segment illustrate parameter passing using register.	05	L2	CO2
	c.	Explain various assembler directives used in assembly language program.	05	L2	CO2
		OR			
Q.4	a.	Explain stack operation with an example.	10	L2	CO2
	b.	Explain the shift and rotate operations with examples.	06	L2	CO2
	c.	Write a program to add 'n' number using indirect addressing mode.	04	L3	CO2
		Module – 3			
Q.5	a.	Showing the possible registers configuration in I/O interface. Explain program controlled input/output.	10	L2	CO3
	b.	Explain in detail the situations where a number of devices capable of initiating interrupts are connected to processor. How to resolve the problems?	10	L2	CO3
		OR			
Q.6	a.	What is an interrupt? With an example illustrate the concept of interrupt.	10	L2	CO3
	b.	Explain the Register involved in a DMA interface to illustrate DMA.	10	L2	CO3
		Module – 4			
Q.7	a.	Illustrate internal structure of static memory.	10	L2	CO4
	b.	With a neat diagram, explain virtual memory organization.	10	L2	CO4
		OR			
Q.8	a.	Classify memory in a computer. With a neat diagram, describe the organization of 2M × 8 DRAM chip.	10	L2	CO4
	b.	Briefly explain secondary storage devices.	06	L2	CO4
	c.	Explain use of a cache memory.	04	L2	CO4

Module – 5					
Q.9	**a.**	List different ways of improving CPU performance. With a neat diagram, discuss three-bus organization of CPU.	**10**	**L2**	**CO5**
	b.	Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z_{in} control signal.	**10**	**L3**	**CO5**
OR					
Q.10	**a.**	Explain single-bus organization of data path in a processor with neat diagram, highlight the importance of gating signals.	**10**	**L2**	**CO5**
	b.	Develop the complete control signal sequence for the instruction Add(R_1), R_3 with appropriate remarks.	**06**	**L3**	**CO5**
	c.	Discuss micro programmed control unit design with relevant diagrams.	**04**	**L2**	**CO5**

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