CBCS SCHEME

USN | | | | | | | | | | |

BEC306C

Third Semester B.E./B.Tech. Degree Supplementary Examination, June/July 2024

Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat block diagram, explain the basic functional units of a computer.	7	L2	CO1
	b.	Explain straight line sequencing. Build a program to add A + B to form C.	6	L3	CO1
	c.	Illustrate big endian and little endian byte addressability.	7	L2	CO1
		OR			
Q.2	a.	Draw the single bus structure and explain the same.	7	L2	CO1
	b.	Explain the connection between processor and memory with neat diagram.	7	L2	CO1
	c.	List the different systems used to represent signed numbers. Solve any two of the following operations on the 8 bit signed number using 2's complement representation. (i) +2, +3 (Addition) (ii) +4, -6 (Addition) (iii) -5, -2 (Addition) (iv) +7, -3 (Addition)	6	L3	CO1
		Module – 2			
Q.3	a.	What is an addressing mode? Explain any five types of addressing modes with examples.	12	L2	CO2
	b.	What is subroutine linkage? Explain with an example subroutine linkage using linkage register. Develop a program to add N numbers by calling parameters by register.	8	L3	CO2
		OR			
Q.4	a.	Illustrate how PUSH and POP operations are performed with an example. Builds a program for safe PUSH and safe POP operations.	10	L3	CO2
	b.	Analyze the following instructions and find the values of R_1, R_2 and R_3 after the execution by considering the initial values of $R_1 = 10101011$, $R_2 = 11001100$, $R_3 = 11100001$, $R_4 = 11000110$, $R_5 = 01011010$ and CY = 1 (i) Lshiftb #3, R_1 (ii) LshiftR #3, R_2 (iii) AshiftR #1, R3 (iv) RotateRC, #2, R4 (v) RotateLC #2, R5	10	L3	CO2
		Module – 3			
Q.5	a.	With a neat diagram, explain I/O interface for an input device.	7	L2	CO3
	b.	Explain the following with respect to interrupts, (i) Vectored interrupts (ii) Interrupt nesting	6	L2	CO3

	c.	With supporting diagram, how multiple priority scheme can be implemented by using separate interrupt request and interrupt acknowledge line for each device.	7	L2	CO3
		OR			
Q.6	a.	Explain how PMA is taking place in the system with relevant diagram.	10	L2	CO3
	b.	Explain basic I/O operations Build a program that neads a line of characters and display it.	10	L2	CO3
		Module – 4			
Q.7	a.	Define : (i) Memory latency (ii) Memory bandwidth (iii) Hit rate (iv) Miss penalty	8	L2	CO4
	b.	Construct an internal organization of $2M \times 8$ dynamic memory chip and explain the same.	12	L3	CO4
		OR			
Q.8	a.	Demonstrate how $1K \times 1$ memory chip is assessed using relevant diagrams.	10	L2	CO4
	b.	With neat diagram demonstrate read and write operations of basic SRAM.	10	L2	CO4
		Module – 5			
Q.9	a.	Discuss the control sequence for execution of instruction ADD (R_3), R_1	8	L2	CO5
	b.	Discuss the control sequence for the instruction ADD R_4, R_5, R_6 for the three bus organization.	12	L2	CO5
		OR			
Q.10	a.	What do you mean by micro instruction? Explain basic organization of microprogram control unit. Construct the sequence of microinstructions for the instruction ADD (R_3), R_1	10	L3	CO5
	b.	Describe single bus organization of data path inside the processor.	10	L2	CO5

* * * * *