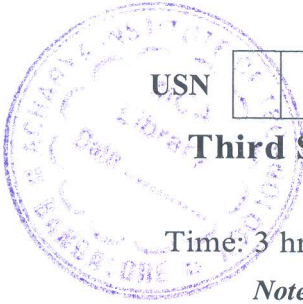


CBCS SCHEME



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BEC306C

Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.*

| Module – 1 | | | M | L | C |
|-------------------|----|--|----|----|-----|
| Q.1 | a. | Explain the basic operational concepts of a computing system. With a neat diagram. | 8 | L2 | CO1 |
| | b. | Explain the various performance parameters effecting the performance of a computer and also provide the basic performance equation. | 8 | L2 | CO1 |
| | c. | Perform the following using 2's complement arithmetic. Use 5 bit representation. State whether overflow flag is set or not with justification i) -17 +18 ii) -27 – 30. | 4 | L3 | CO1 |
| OR | | | | | |
| Q.2 | a. | Explain Big-Endian and Little Endian assignments. | 6 | L2 | CO1 |
| | b. | Consider a computer that has a byte addressable memory organized 32-bit words according to a big endian scheme. A program reads ASCII characters entered by a keyboard and store them in successive byte locations starting at location 1000. Show the contents of the two memory words "JOHNSON". Repeat the same of little endian scheme. [NOTE : ASCII code for JOHNSON : 4A, 4F, 4E, 53, 4F, 4E.] | 4 | L3 | CO1 |
| | c. | Explain the following with illustrations i) Three address instruction ii) Two address instruction iii) One address instruction iv) Zero address instruction | 10 | L2 | CO1 |
| Module – 2 | | | | | |
| Q.3 | a. | Define addressing mode. List the various addressing modes. | 6 | L1 | CO2 |
| | b. | Registers R1 and R2 of a computer contain the decimal values 1200 and 1400. What is the effective address of the memory open and in each of the following instructions? i) Load 20(R12), (R5) ii) Move #3000, R5 iii) Store R5, 30(R1, R2) iv) Add – (R2), R5 v) Subtract (R1) + R5. | 10 | L3 | CO2 |
| | c. | Write a short sequence, of machine instructions for the task : "Add the contents of memory location A to those of B and place the answer in location C. Instructions Loads LOC, R _i and store R _i , LOC are available for data transfer and Add instruction is available for addition. | 4 | L3 | CO2 |
| OR | | | | | |
| Q.4 | a. | Explain the concept of stack and Queues with an example. | 6 | L2 | CO2 |
| | b. | What are assembler directives? Explain various assembler directives with an example. | 8 | L2 | CO2 |

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|-------------------|----|---|----|------|-------|
| | c. | Write a program to check whether the given byte is odd or even. If add, store a byte '0' in location 1001 and else store a byte '1' in location 1001. Data is available in location 1000. | 6 | L3 | CO2 |
| Module – 3 | | | | | |
| Q.5 | a. | Define Interrupts. Explain Daisy chain and priority structure methods of handling interrupts from multiple devices. | 10 | L1,2 | CO3 |
| | b. | Explain various ways of accessing I/O devices. | 6 | L2 | CO3 |
| | c. | Differentiate memory mapped I/O and I/O mapped I/O. | 4 | L1 | CO3 |
| OR | | | | | |
| Q.6 | a. | Write a program that reads one line from keyboard, stores it in buffer and echos it back to display. | 6 | L3 | CO3 |
| | b. | Explain how vectored interrupts are handled by array processor in general. | 6 | L2 | CO3 |
| | c. | Explain Direct memory access control. | 8 | L2 | CO3 |
| Module – 4 | | | | | |
| Q.7 | a. | Define : i) Memory Access time ii) Memory cycle time iii) MFC signal iv) Virtual or logical address. | 4 | L1 | CO4 |
| | b. | With a neat diagram, explain the working principle of magnetic disk. | 6 | L2 | CO4 |
| | c. | With a neat diagram, explain internal organization of 16 × 8 memory organization. | 10 | L2 | CO4 |
| OR | | | | | |
| Q.8 | a. | Discuss the concept of cache memory. | 6 | L3 | CO4 |
| | b. | With a neat diagrams, explain internal memory organization of a 2m × 8 dynamic memory chip. | 8 | L2 | CO4 |
| | c. | Explain the concept of virtual memory. | 6 | L2 | CO4 W |
| Module – 5 | | | | | |
| Q.9 | a. | With a neat diagram, explain single bus organization of the data path inside a processor. | 8 | L2 | CO5 |
| | b. | Discuss the hard wired control unit. | 6 | L3 | CO5 |
| | c. | With a neat sketch, explain micro-programmed control unit. | 6 | L2 | CO5 |
| OR | | | | | |
| Q.10 | a. | Explain three – Bus organization of data path. | 8 | L2 | CO5 |
| | b. | Write and discuss the instruction ADD (R3), R1. | 6 | L3 | CO5 |
| | c. | Discuss the organization of a control unit to allow conditional branching in the microprogram. | 6 | L3 | CO5 |
