CBCS SCHEME

USN | | | | | | | | | | |

18EC56

Fifth Semester B.E. Degree Examination, June/July 2024
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. List the importance of HDL. **(04 Marks)**

b. Explain design flow for designing VLSI IC circuits with a neat flow chart. **(10 Marks)**

c. Discuss the different levels of abstraction used in verilog modelling and write example in each case. **(06 Marks)**

OR

2 a. Describe the top down design approach with 4-bit ripple counter example. **(12 Marks)**

b. What is the need of stimulus block in simulation? Discuss different techniques of applying stimulus. **(08 Marks)**

Module-2

3 a. List all the data types of verilog HDL. Explain any 4 with example. **(10 Marks)**

b. Write a verilog description of SR latch and write a stimulus code, use $monitor to display the simulation time, inputs and outputs. **(06 Marks)**

c. Describe different methods of connecting ports to external signals. **(04 Marks)**

OR

4 a. Write verilog statements to declare the following variables.

i) Declare a 16-bit vector called addr

ii) Declare a memory RAM with 1K bytes

iii) Declare a constant port_id = 5

iv) Declare time variable T_1. **(04 Marks)**

b. Discuss any 4 system tasks with example. **(08 Marks)**

c. Bring out differences between :

i) $display ii) $monitor iii) Sized and unsized data. **(08 Marks)**

Module-3

5 a. Design a 4-bit ripple carry adder using 1-bit full adder. **(08 Marks)**

b. What is the output of the following expressions, given :

a = 4′ b1010 b = 4′ b1011 c = 4′ b110x

i) a = = = 6

ii) y = ∧ b

iii) y = a && b

iv) y = b >>>1

v) y = {2a[1], b, 11, c[3]}

vi) y = a ¦ b. **(06 Marks)**

c. Write a verilog program to implement 4 × 1 MUX using :

i) Conditional operator

ii) Data flow Boolean expressions. **(06 Marks)**

OR

6 a. Derive Boolean expressions for 4-bit carry look ahead adder and also write the design module. **(10 Marks)**

b. Design a 2 × 1 MUX by writing logic circuit using bufifo and bufifi for the following delay specification.

	Min	typ	Max
Rise	3	4	5
Fall	6	7	9
Turn off	5	6	7

(04 Marks)

c. Write verilog module, test bench and waveform for the circuit shown in Fig.Q6(c). Assume
t = 0, a = 0, b = 0, c = 0, d = 0
t = 5, a = 1, b = 1, c = 1, d = 1
t = 15, a = 0, c = 0.

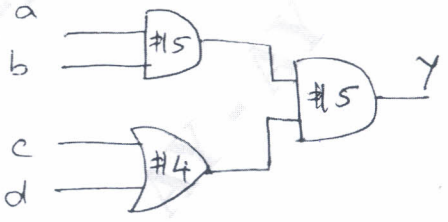

Fig.Q6(c) **(06 Marks)**

Module-4

7 a. Differentiate always initial blocking and on blocking statement. **(08 Marks)**

b. Write a verilog program to call a function called calc – parity which computes the parity of a 32 – bit data [31 : 0] Data and display the parity. **(06 Marks)**

c. Explain the following control statements :
i) case ii) for loop. **(06 Marks)**

OR

8 a. Bring out differences between tasks and functions of verilog. **(06 Marks)**

b. Write a verilog program for 1 × 4 demux considering 0, 1, x, z values for select inputs. **(08 Marks)**

c. Explain the different event – based timing control with example. **(06 Marks)**

Module-5

9 a. Define the term logic synthesis. With a neat block diagram. Explain computer aided logic synthesis process. **(08 Marks)**

b. Discuss conditional execution with an example. **(08 Marks)**

c. Bring out difference between $strobe and $display. **(04 Marks)**

OR

10 a. What will the following statements translate to when run on a logic synthesis tool?
i) assign y = (a & b) ¦ (c & d) where a, b, c, d are 2–bit vectors
ii) if(s) out = i1 ;
else out = i0 ; **(06 Marks)**

b. Explain force and release procedural assignments with example. **(08 Marks)**

c. Discuss any 4 system tasks related to files. **(06 Marks)**

* * * * *