CBCS SCHEME

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18EC644

Sixth Semester B.E. Degree Examination, June/July 2024
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain logic level evolution in real-world circuits and define the term V_{OL}, V_{OH}, V_{IL} and V_{IH}. **(08 Marks)**

b. Explain simple methodology followed in IC industries with block diagram. **(08 Marks)**

c. Express the number $(4.5)_d$ in floating – point format with 5 bits of exponent and 12 bits of mantissa magnitude. **(04 Marks)**

OR

2 a. Develop a datapath to perform a multiplication of two complex numbers. The real and imaginary parts of the operands are represented as signed fixed-point numbers with 4 pre-binary-point and 12 post-binary-point bits. The real and imaginary parts of the products are similarly represented, but with 8 pre-binary-point and 24 post-binary points. **(08 Marks)**

b. Explain BCD code and 7-segment decoder and also write verilog model for that. **(08 Marks)**

c. Explain testbench and design under verification with proper diagram. **(04 Marks)**

Module-2

3 a. Explain basics of memory concept with proper symbol and calculate how many address lines and data lines are required for bellow memory size:
i) 64KB ii) 512MB **(08 Marks)**

b. Design 64K × 8 composite memory using 16K × 8 component. Note: Use common data input and output. **(08 Marks)**

c. List out difference between SRAM and DRAM. **(04 Marks)**

OR

4 a. Explain multi-port memory. List out advantages and disadvantages. Develop a verilog model of a dual-port. 4K × 16 – bit flow-through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(08 Marks)**

b. Explain error detection and correction and also compute the 12-bit ECC word corresponding to the 8-bit data word 01010101. **(08 Marks)**

c. Explain pipelined SSRAM. **(04 Marks)**

Module-3

5 a. What is PLD? Explain the internal circuit of a PAL16L8 component. Specify the difference between PAL16L8 and PAL16R8. **(08 Marks)**

b. Explain output logic macrocell of a GAL22V10 component. Design priority encoder that has 08 inputs. The design is to be implemented in GAL22V10 component. **(08 Marks)**

c. Explain application specific integrated circuits. **(04 Marks)**

OR

6	a.	Explain Xilinx Spartan-II FPGA logic block.	**(08 Marks)**
	b.	Explain packaging and circuit boards.	**(08 Marks)**
	c.	Explain differential signaling.	**(04 Marks)**

Module-4

7	a.	Explain the serial transmission of 64 bit data with suitable timing diagram.	**(08 Marks)**
	b.	Explain Flash ADC and successive approximation ADC with diagram.	**(08 Marks)**
	c.	Explain Firewire serial interface standards.	**(04 Marks)**

OR

8	a.	Explain polling and interrupts.	**(08 Marks)**
	b.	Explain Gumnut I/O write and read operations with timing diagram.	**(08 Marks)**
	c.	What are the purpose of control register and status register in I/O controller?	**(04 Marks)**

Module-5

9	a.	Explain prototypical design flow, including hardware/software co-design.	**(10 Marks)**
	b.	What is design optimization? Explain optimization of area and power.	**(10 Marks)**

OR

10	a.	Explain Built-In-Self-Test (BIST) technique.	**(10 Marks)**
	b.	Briefly explain following:	
		i) Fault models and fault simulation.	
		ii) Scan design and boundary scan.	**(10 Marks)**

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