CBCS SCHEME

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21EC63

Sixth Semester B.E. Degree Examination, June/July 2024
VLSI Design and Testing

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. State Moore's law, elaborate with graph. **(04 Marks)**

b. Derive the expression for drain current in linear and saturation regions. **(10 Marks)**

c. Explain the following non-ideal characteristics:
i) Body effect ii) Channel length modulation. **(06 Marks)**

OR

2 a. Explain working of nMOS enhancement mode transistor operation with neat sketches and relevant equations. **(08 Marks)**

b. Draw inverter circuit and explain its DC transfer characteristics. **(08 Marks)**

c. Draw the schematic of
i) $F = \overline{A + BC}$ ii) $F = \overline{AB + CD}$. **(04 Marks)**

Module-2

3 a. Explain CMOS fabrication process with necessary diagrams. **(10 Marks)**

b. With relevant equations explain transient response of CMOS inverter. **(05 Marks)**

c. With neat diagrams explain layout design rules. **(05 Marks)**

OR

4 a. Draw the stick diagram and layout of three input NAND gate. **(06 Marks)**

b. Find maximum and minimum rise time and fall time delays of two input NAND gate. **(06 Marks)**

c. Estimate the minimum delay of the path from A to B in Fig.Q.4(c) and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on the input and the output load is equivalent to 45λ of transistor width.

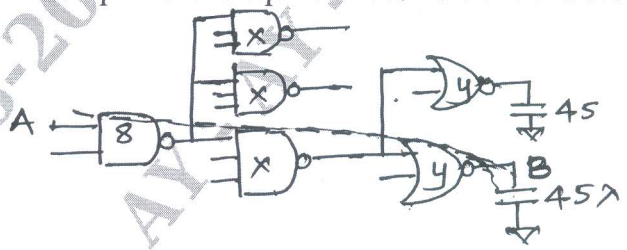

Fig.Q.4(c)

(08 Marks)

Module-3

5 a. Explain the operation of three transistor DRAM cell with necessary timing diagrams. **(08 Marks)**

b. Draw the structure of NAND flash memory cell and explain the operation. **(06 Marks)**

c. Explain ferroelectric RAM with necessary diagrams. **(06 Marks)**

OR

6 a. Explain read and write operations of SRAM cell with necessary diagrams. **(08 Marks)**

b. What is row decoder? Explain with an example. **(06 Marks)**

c. Explain data programming and erasing methods of flash memory. **(06 Marks)**

Module-4

7 a. Briefly explain different types of faults in digital circuits. **(08 Marks)**

b. Consider the logic circuit shown in Fig.Q.7(b) find Boolean difference with respect to x_3.

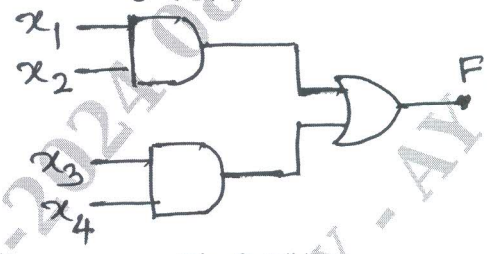

Fig.Q.7(b)

(06 Marks)

c. Explain detection of multiple faults in combinational logic circuits. **(06 Marks)**

OR

8 a. With neat sketch, explain path oriented decision making algorithm. **(10 Marks)**

b. For a given logic network determine tests for checking all single node faults (Fig.Q.8(b))

$F = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$ **(10 Marks)**

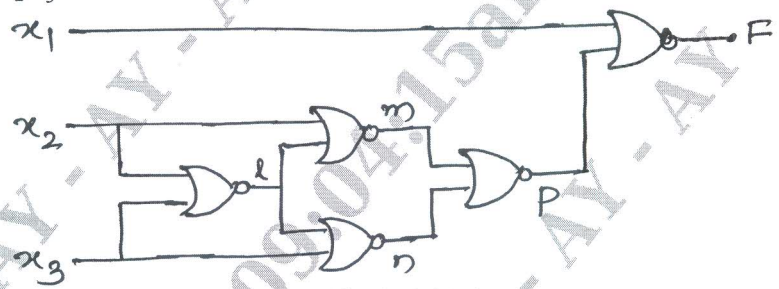

Fig.Q.8(b)

Module-5

9 a. Briefly explain :

i) Controllability ii) Observability. **(06 Marks)**

b. Explain adhoc design rules for improving testability. **(06 Marks)**

c. With neat diagram explain partial scan. **(08 Marks)**

OR

10 a. List LSSD design rules. **(10 Marks)**

b. Explain test generation based on functional fault models. **(10 Marks)**

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