USN 1 A 7 2 3 M T 4 0 5

BMT302

Third Semester B.E./B.Tech. Degree Supplementary Examination, June/July 2024

Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M: Marks, L: Bloom's level, C: Course outcomes.

		Module – 1	M	L	С
Q.1	a.	Define filter and write the advantages of active filter over passive filter.	10	L1	CO1
	b.	With neat circuit diagram, derive the expression for gain of first order high pass filter and also plot frequency response curve.	10	L3	CO1
		OR			
Q.2	a.	Define band pass filter and write about wide band pass filter.	10	L1	CO1
	b.	With neat circuit diagram and frequency response plot write about wide band reject filter.	10	L3	COI
	L	Module – 2			
Q.3	a.	Define oscillator and write about the principle of oscillation.	10	L1	CO2
	b.	With neat sketch, write about the working of RC phase shift oscillator.	10	L3	CO2
		OR			
Q.4	a.	Define comparator and write about the operation of non inverting comparator.	10	L1	CO2
	b.	With neat sketch and relevant waveforms write about Schmitt trigger.	10	L3	CO2
		Module – 3			
Q.5	a.	Explain the application of astable multivibrator as square wave oscillator.	10	L2	CO5
	b.	Develop a circuit to realize the operation of 555 timer as monostable multivibrator.	10	L3	CO5
		OR			
Q.6	a.	Explain the application of monostable multi-vibrator as frequency divider.	10	L2	CO5
	b.	Develop a circuit to realize the operation of 555 timer as a stable multivibrator.	10	L3	COS
		Module – 4			
Q.7	a.	Implement a half adder circuit and also implement a full adder circuit using two half adders.	10	L3	CO4
	b.	Develop half and full adder using basic gates, universal gates and write the truth table of operation.	10	L3	CO4
	1	OR			
Q.8	a.	Explain multiplexer and write about 2:1 MUX using basic gates.	10	L2	CO ₄
	b.	Explain demultiplexer and write about 1:4 DEMUX with relevant details.	10	L2	CO4

	Module – 5	15		
a.	Explain the operation of RS flip flop using NOR gates.	10	L2	CO6
b.	Develop a two bit synchronous binary counter using JK flip flops.	10	L3	CO6
1	OR			
a.	Explain the operation of D flip flop using NAND gates.	10	L2	CO6
b.	Develop a three bit synchronous binary up counter using JK flip flops.	10	L3	CO6
	a.	 a. Explain the operation of RS flip flop using NOR gates. b. Develop a two bit synchronous binary counter using JK flip flops. OR	 a. Explain the operation of RS flip flop using NOR gates. b. Develop a two bit synchronous binary counter using JK flip flops. OR a. Explain the operation of D flip flop using NAND gates. 10 	 a. Explain the operation of RS flip flop using NOR gates. b. Develop a two bit synchronous binary counter using JK flip flops. DR a. Explain the operation of D flip flop using NAND gates. 10 L2 10 L2

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