CBCS SCHEME

USN | | | | | | | | | | |

18MT35

Third Semester B.E. Degree Examination, Dec.2024/Jan.2025
Analog and Digital Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define clipper construct a double ended clipper to clip the output at +3V and –2V from 10V (P – P) supply voltage. **(08 Marks)**

b. Define filter. Mention the advantages of active filters over passive filters. Also with a neat sketch explain the operation of first order active low pass filter and derive the expression for gain. **(12 Marks)**

OR

2 a. With a neat sketch, explain the operation of notch filter. Also mention its application. **(10 Marks)**

b. Design a wide band pass filter with cut off frequencies 200Hz and 1KHz and pass band gain = 4. Also calculate quality factor. **(10 Marks)**

Module-2

3 a. Design and explain the working of RC phase shift oscillator for f_0 = 200Hz. **(10 Marks)**

b. What is an oscillator? Mention the conditions required for sustained oscillation and also explain the working of Wein bridge oscillator. **(10 Marks)**

OR

4 a. What is comparator? With a neat diagram and waveform explain zero crossing detector. **(10 Marks)**

b. Explain the working of inverting comparator as Schmitt trigger with necessary waveforms. **(10 Marks)**

Module-3

5 a. In detail explain pin diagram and internal architecture of 555 timer. **(10 Marks)**

b. Explain the operation of 555 timer as monostable multivibrator with help of circuit diagram and waveform. **(10 Marks)**

OR

6 a. Explain the operation of 555 timer as Astable multivibrator with the help of circuit diagram and waveform. **(10 Marks)**

b. With neat diagram explain any two applications of astable multivibrator. **(10 Marks)**

Module-4

7 a. Using K – Map solve.

i) $P = f(r, s, t, u) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$

ii) $G = f(a, b, c, d) = \pi(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$. **(06 Marks)**

b. Implement $f(A, B, C) = \Sigma m(1, 3, 5, 6)$ using 4 : 1 MUX. **(06 Marks)**

c. Explain with logic diagram and truth table the full adder circuit. Also implement full adder using two 4 : 1 MUX. **(08 Marks)**

OR

8 a. What is a decoder? With logic diagram and truth table explain 3 to 8 line decoder. **(08 Marks)**

b. Design BCD to decimal decoder circuit. **(08 Marks)**

c. Implement full adder circuit using decoder and two OR gates. **(04 Marks)**

Module-5

9 a. With the neat circuit derive the characteristic equation for the following :

i) Clocked D flip-flop

ii) Clocked JK flip-flop. **(12 Marks)**

b. Design a 3 bit binary ripple up counter. **(08 Marks)**

OR

10 a. Implement a BCD ripple counter. **(12 Marks)**

b. Design a 3 bit synchronous binary up counter. **(08 Marks)**

* * * * *