CBCS SCHEME

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BMT302

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: **1.** ***Answer any FIVE full questions, choosing ONE full question from each module.***
2. ***M : Marks , L: Bloom's level , C: Course outcomes.***

		Module – 1	M	L	C
Q.1	a.	List the commonly used filters and compare between the advantages of active and passive filters.	6	L1	CO1
	b.	Plot the frequency response of the major active filters.	8	L1	CO1
	c.	Explain the steps involved in first order low-pass filter design.	6	L2	CO1
		OR			
Q.2	a.	With a neat circuit, explain the working of second order Low-pass Butterworth filter.	10	L2	CO1
	b.	Design a Band-pass filter and show and relationship between Quality factor (Q) and Bandwidth (BW) for the center frequency.	10	L3	CO1
		Module – 2			
Q.3	a.	Mention the major types of oscillators and explain the significance of frequency stability in oscillators.	10	L2	CO2
	b.	Design a phase shift oscillator with C = 0.1μF, R_1 = 33kΩ, R_f = 1mΩ, R = 3.3kΩ, so that the generated frequency f_0 = 200Hz. Draw the circuit and mark the values.	10	L3	CO2
		OR			
Q.4	a.	With a neat Schematic, explain the working of non-inverting comparator and plot the output waveforms.	10	L2	CO2
	b.	Derive an expression for hysteresis voltage (V_{hy}) in an inverting comparator as Schmitt trigger and plot the hysteresis curve.	10	L3	CO2
		Module – 3			
Q.5	a.	Draw and explain the pin configuration of 555-timer connection diagram.	10	L1	CO3
	b.	List the application of monostable multivibrator. Estimate the value of 'R_A' in monostable multivirbrator used as a divide by network. If the frequency of the input trigger signal is 2KHz and C = 0.01μF.	10	L3	CO3
		OR			
Q.6	a.	Derive an expression for duty cycle for the Astable multivibrator and plot capacitor and output voltage waveforms.	10	L3	CO3

	b.	Determine the positive pulse width t_c negative pulse width t_d and free running frequency 'f_0'. In an astable multivibrator with the following value $R_A = 2.2K\Omega$, $R_B = 3.9K\Omega$ and $C = 0.1\mu F$.	**10**	**L3**	**CO3**
		Module – 4			
Q.7	**a.**	Implement full adder in Sum Of Products (SOP) form and using two half adders with sum and carry expressions.	**10**	**L2**	**CO4**
	b.	Implement Quadruple 2*0-1 line multiplexer with function table.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Realize octal – to – binary encoder using basic gates and write the truth table to implement the same.	**10**	**L2**	**CO4**
	b.	Realize BCD – to – decimal decoder using basic gates and write truth tale to implement the same.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Illustrate the working of D-Flip-Flop with a neat logic diagram and excitation table.	**10**	**L2**	**CO5**
	b.	Draw and outline the working of 4-bit synchronous counter.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain clocked JK-Flip-flop with a neat logic diagram and characteristics equation.	**10**	**L2**	**CO5**
	b.	Design a BCD ripple counter with the following : i) Logic diagram ii) State diagram iii) Timing diagram.	**10**	**L2**	**CO5**

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