CBCS SCHEME

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BMT304

# Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
## Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

***Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.***
***2. M : Marks , L: Bloom's level , C: Course outcomes.***

| | | Module – 1 | M | L | C |
|---|---|---|---|---|---|
| Q.1 | a. | Draw and explain the connection between memory and processor with the respective registers. | 8 | L2 | CO1 |
| | b. | Explain in brief different types of key parameters that affect the processor performance. | 8 | L2 | CO1 |
| | c. | Explain Big-endian and Little-endian method with neat diagram. | 4 | L2 | CO1 |
| | | **OR** | | | |
| Q.2 | a. | Explain branching concept by considering example of adding 'n' numbers using straight line program and using loop. | 8 | L3 | CO1 |
| | b. | Perform the following arithmetic operations using 5-bit 2's complement number system :<br>i) A + B ii) A – B iii) –A + B iv) –A – B where A = – 7 and B – 12. | 8 | L3 | CO1 |
| | c. | Discuss with block diagram basic functional units of a computer. | 4 | L2 | CO1 |
| | | **Module – 2** | | | |
| Q.3 | a. | Explain with example the following addressing modes :<br>i) Indirect mode ii) Indexing mode. | 10 | L2 | CO1 |
| | b. | Explain shift and rotate instruction with example. | 10 | L2 | CO1 |
| | | **OR** | | | |
| Q.4 | a. | Discuss the following in case of sub routine :<br>i) Subroutine nesting ii) Parameter passing. | 10 | L3 | CO1 |
| | b. | Explain PUSH and POP instruction with example. | 10 | L2 | CO1 |
| | | **Module – 3** | | | |
| Q.5 | a. | Explain any two methods of handling multiple devices using interrupt priority schemes. | 10 | L2 | CO2 |
| | b. | Explain how simultaneous interrupt request from several I/O devices will be handled by a processor through a single INTR line. | 10 | L2 | CO2 |
| | | **OR** | | | |
| Q.6 | a. | Explain the DMA concept in detail. | 10 | L2 | CO2 |
| | b. | Define Bus arbitration. Explain two approaches of bus arbitration. | 10 | L1 | CO2 |
| | | **Module – 4** | | | |
| Q.7 | a. | Discuss the internal organization of a 2M × 8 asynchronous DRAM chip. | 10 | L3 | CO3 |
| | b. | Explain with short description any four non-volatile memory concepts. | 10 | L2 | CO3 |
| | | **OR** | | | |
| Q.8 | a. | Draw a neat diagram 16 × 8 bit organized 1 K × 1 memory chip. Explain the read and write operation of the memory. | 10 | L3 | CO3 |
| | b. | What is virtual memory? Explain virtual memory organization with a neat diagram. | 10 | L3 | CO3 |
| | | **Module – 5** | | | |
| Q.9 | a. | Write the single bus organization of the data paths inside a processor and explain the importance of each unit. | 10 | L2 | CO4 |
| | b. | List the control sequence of execution of Add(R3), R1 instruction. | 10 | L3 | CO4 |
| | | **OR** | | | |
| Q.10 | a. | Discuss micro instruction sequencing organization in micro programmed control unit. | 10 | L3 | CO4 |
| | b. | Explain with neat sketch hardwired control unit organization. | 10 | L2 | CO4 |

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