

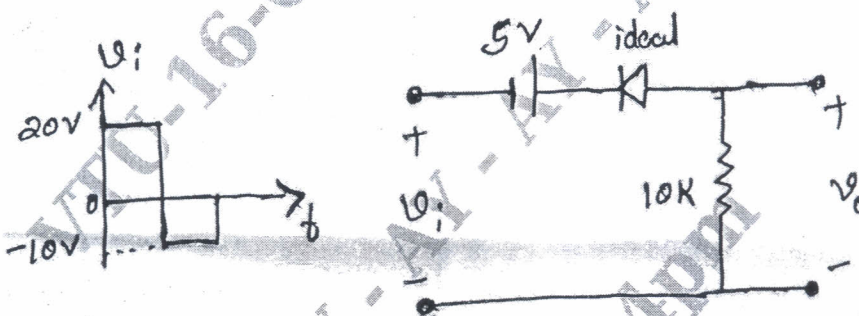
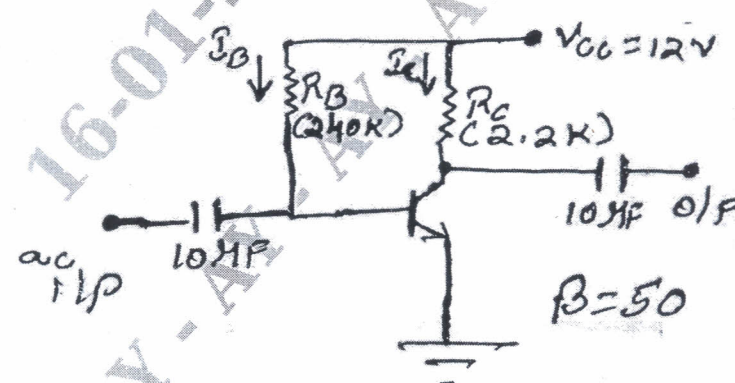
Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Analog Electronic Circuits

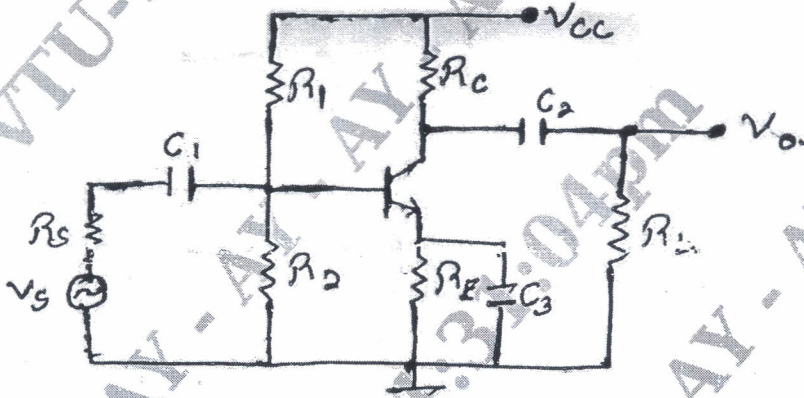
Time: 3 hrs.

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.

2. M : Marks , L: Bloom's level , C: Course outcomes.

Module - 1			M	L	C
Q.1	a.	Explain the operation of positive shunt clipper.	8	L2	CO1
	b.	Derive an expression for the stability factor $S_{(V_{BE})}$ and $S_{(I_{CO})}$ for fixed bias circuit.	6	L3	CO1
	c.	For the circuit shown in Fig Q1(c), sketch the output voltage waveform.	6	L3	CO1
 Fig Q1 (c)					
OR					
Q.2	a.	With circuit diagram, explain voltage divider biasing circuit. Also derive the I_B and V_{CE} .	8	L2,3	CO1
	b.	Draw and explain the working of negatives peak clamper.	6	L1,2	CO1
	c.	Determine the following for the fixed bias configuration shown in Fig Q2(c). i) I_{BQ} and I_{CQ} ii) V_{CEQ} iii) V_B and V_C iv) V_{BC}	6	L3	CO1
 Fig Q2(c)					

Module – 2					
Q.3	a.	State and prove dual of miller's theorem.	6	L1,4	CO2
	b.	Define h-parameters. Draw the h-parameter model of a transistor in CE mode.	6	L1,2	CO2
	c.	Obtain midband analysis of BJT single stage amplifier. Derive expression for current gain and input impedance.	8	L3,4	CO2
OR					
Q.4	a.	Mention various capacitors effects on frequency response. Derive equations for miller input capacitors and miller output capacitance.	10	L1,3	CO2
	b.	Consider a single stage CE amplifier with $R_s = 1K$, $R_1 = 50K$, $R_2 = 2K$, $R_c = 2K$, $R_L = 2K$, $h_{fe} = 50$, $h_{ie} = 1.1K$, $h_{oe} = 25 \mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$ as shown in Fig Q4(b). Find A_i , R_i , R_o , A_v .	10	L3	CO2
 Fig Q4(b)					
Module – 3					
Q.5	a.	Explain the need of a cascading amplifier. Draw and explain to block diagram of two stage cascade amplifier.	8	L2	CO3
	b.	For voltage series feedback amplifier, derive an expression for input impedance and output impedance.	8	L3	CO3
	c.	A feedback amplifier has a gain of 1000 without feedback. Find the gain with feedback for a negative feedback of 10% (gain in dB).	4	L3	CO3
OR					
Q.6	a.	Draw a feedback amplifier in block diagram form. Identify each block and explain its function.	10	L1,2	CO3

	b. For the Darlington emitter – follower shown in Fig Q6(b), calculate - The DC bias voltage V_B, V_E, V_C and current and I_B and I_C - The input and output impedances - The voltage and current gains - The ac output voltage for $V_i = 120\text{mV}$.	10	L3	CO3
Module – 4				
Q.7	a. Analyze the working of series fed directly coupled class A power amplifier with respect to efficiency.	8	L4	CO4
	b. Design the component values of wein bridge oscillator of Fig Q7(b) for a frequency of oscillations of 4 KHz.	4	L4	CO4
Fig Q7(b)				
	c. Explain the characteristics of crystal with neat diagram, explain the crystal oscillation in series resonances circuit.	8	L2	CO4
OR				
Q.8	a. Examine the basic principle of oscillators.	6	L4	CO4
	b. An ideal class B push pull power amplifier with input is output transformers has $V_{cc} = 20\text{V}$, $N_2 = 2N_1$ and $R_L = 20\Omega$. The transistors has $h_{FE} = 20$. Let the input be sinusoidal. For maximum output signal at $V_{CE(P)} = V_{CC}$. Determine: - The output signal power - The collector dissipation in each transistor - Conversion efficiency	6	L3	CO4

	c.	Discuss the different types of power amplifiers.	8	L4	CO4
Module – 5					
Q.9	a.	Explain the basic operation and characteristics of n-channel depletion type MOSFET.	10	L2	CO4
	b.	Derive expression for z_i , z_o , A_v for voltage divider bias circuit using FET.	10	L3	CO4
OR					
Q.10	a.	With neat diagram, explain the construction of n channel JFET.	10	L2	CO5
	b.	Data sheet for a JFET indicates that $I_{DSS} = 10\text{mA}$ and $V_{GS(off)} = -4\text{V}$. Determine the drain current for $V_{GS} = 0\text{V}$, -1V and -4V .	6	L3	CO5
	c.	Discuss the difference between JFET and MOSFET.	4	L4	CO5
