CBCS SCHEME

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18EE35

Third Semester B.E. Degree Examination, Dec.2024/Jan.2025
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Deduce the following in the proper canonical form as mentioned :
i) $F = AB + \overline{C}D + A\overline{B}C$ into standard SOP form
ii) $Z = Wo(W + X + Y)$ into standard SOP form. **(10 Marks)**

b. Reduce the following expression using K –map and implement the same using basic gates.
i) $f(a, b, c, d) = \sum m(3, 4, 6, 9, 11, 12, 13, 14, 15)$
ii) $f(a, b, c, d) = \Pi m\ (0, 2, 4, 5, 6, 7, 9, 11)$. **(10 Marks)**

OR

2 a. Simplify $f(a, b, c, d) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$ using Quine-McClusky method, find prime implicants and essential prime implicants. **(12 Marks)**

b. Reduce the following boolean expression using 5 variable K-map
$f(a, b, c, d, e) = \sum m(0, 2, 4, 5, 6, 7, 13, 15, 16, 18, 20, 21, 22, 23, 29, 31)$. **(08 Marks)**

Module-2

3 a. Design a combinational circuit to find the 9's complement of a single digit BCD number. Realize the equation using logic gates. **(10 Marks)**

b. What is comparator? Design a 2-bit magnitude comparator. **(10 Marks)**

OR

4 a. What is priority encoder? Design 4 input D_0, D_1, D_2 and D_3 encoder with there outputs Y_1, Y_0 and valid input. **(10 Marks)**

b. Implement $F(A, B, C, D) = \overline{A}\overline{B}\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$ using 8 to 1 multiplexer. **(10 Marks)**

Module-3

5 a. Explain the operation of master salve J-K flip-flop with logic diagram, truth table, symbol and timing diagram. **(12 Marks)**

b. Derive the characteristic equation of SR flip-flop, J-K flip-flop, T-flip-flop and D-flip-flop. **(08 Marks)**

OR

6 a. Explain the operation of gated SR flip-flop using NAND logic. **(10 Marks)**

b. Construct T-flip-flop using :
i) J-K flip-flop
ii) SR flip-flop. **(10 Marks)**

Module-4

7 a. Mention the four different modes of shift register. With a neat block diagram, explain parallel in serial out shift register. **(10 Marks)**

b. Design asynchronous 3-bit up/down counter using J-K flip-flop. **(10 Marks)**

OR

8 a. Design synchronous Mod-6 counter using D flip-flop. **(10 Marks)**

b. Explain 4-bit universal shift register using 4 to 1 multiplexer with the help of logic diagram. Write a mode control table. **(10 Marks)**

Module-5

9 a. Distinguish between mealy and Moore model with block diagram. Define state variable and excitation variable. **(10 Marks)**

b. Explain flash memory concept in detail. Mention its advantages and drawbacks. **(10 Marks)**

OR

10 a. What is ROM? What are various types of ROM? Explain. **(10 Marks)**

b. Design a clocked sequential circuit that operates according to the state diagram shown in Fig.Q10(b), implement the circuit using D- flip-flop. **(10 Marks)**

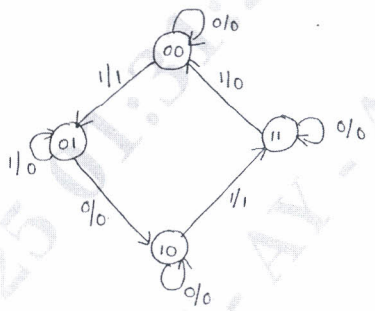

Fig.Q10(b)

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