CBCS SCHEME

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18EE46

Fourth Semester B.E. Degree Examination, Dec.2024/Jan.2025
Operational Amplifiers and Linear ICs

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Standard resistance and capacitance data table may be used.

Module-1

1 a. Explain the ideal characteristics of op-amp. **(04 Marks)**

b. Explain the following terms:
i) Input offset voltage ii) Input offset current iii) CMRR iv) Slew rate. **(08 Marks)**

c. What is an instrumentation amplifier? For instrumentation amplifier using transducer bridge obtain an expression for output voltage V_O interms of change in resistance ΔR of the transducer. Draw the circuit diagram. **(08 Marks)**

OR

2 a. Design a summing amplifier to add three dc voltages. The output of this circuit must be equal to two times the negative sum of the inputs. **(08 Marks)**

b. Design an averaging circuit for four DC voltages. Use non-inverting op-amp configurations. Derive the necessary equations. **(08 Marks)**

c. In the circuit of AC inverting amplifier as shown in Fig.Q.2(c), $R_{in} = 50\Omega$, $C_i = 0.1\mu f$, $R_1 = 100\Omega$, $R_F = 1K\Omega$, $R_L = 10K\Omega$ and supply voltages = $\pm 15V$. Determine the Bandwidth of the amplifier (UGB = 10^6 for 741 op-amp). **(04 Marks)**

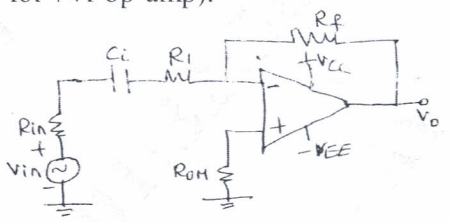

Fig.Q.2(c)

Module-2

3 a. Derive the gain equation for first order low pass butterworth filter. **(08 Marks)**

b. Design a second order high pass filter at a cut-off of 1kHz. **(06 Marks)**

c. Design a wide band pass filter with lower cut-off frequency $f_L = 200Hz$, higher cut-off frequency $f_H = 1kHz$, pass band gain = 4. Assume capacitor values of high pass and low pass sections as 0.05 μf and 0.01 μf respectively. Also calculate Q factor. Draw the circuit and mark the design values. **(06 Marks)**

OR

4 a. Explain the working and design of op-amp voltage follower regulator. **(06 Marks)**

b. Design an adjustable voltage to produce an output of 12V with a maximum load current of 50mA, using a 741 op-amp use a 1N756 zener diode with $V_Z = 8.2V$, $I_Z = 20mA$ and $Z_Z = 8\Omega$. Analyze the circuit designed to find line regulation, load regulation and ripple rejection. **(10 Marks)**

c. Sketch the circuit of vlg regulator using LM317 voltage regulator. Explain the circuit operation. **(04 Marks)**

Module-3

5 a. Design an RC phase shift oscillator for an output frequency of 5kHz. Use LM741 with ±15V supply. **(06 Marks)**

b. A triangular/rectangular signal generator is to be designed to have a 5V peak-to-peak triangular output, a frequency ranging from 200Hz to 2kHz and a duty cycle adjustable from 20% to 80%. Bipolar op-amps with a supply of ±15V are to be used. Determine suitable component value and draw circuit diagram. **(08 Marks)**

c. Explain the working of voltage to current converter with grounded load. **(06 Marks)**

OR

6 a. Explain the working of an inverting voltage comparator circuit. Draw the input, output voltage waveforms when v_{ref} is positive and negative. **(06 Marks)**

b. Using a 741 op-amp with a supply of ±12V, design an inverting Schmitt trigger circuit to have trigger points of ±2V. **(06 Marks)**

c. Draw the circuits to show how diodes may be used to select different trigger points of an inverting Schmitt trigger circuit. Explain its operation and draw relevant input and output waveforms. **(08 Marks)**

Module-4

7 a. Discuss the advantages of a precision rectifier over an ordinary diode circuit and show how voltage gain can be achieved with a precision saturating rectifier. Explain circuit operation. **(06 Marks)**

b. Design a non-saturating precision halfwave rectifier to produce 2V peak output from a sine wave input with a peak value of 0.5V and frequency of 1MHz. Use a bipolar op-amp with a supply voltage of ±15V. **(06 Marks)**

c. Show how half-wave precision rectifier can be combined with a summing circuit to produce a full wave precision rectifier. Draw the voltage waveforms throughout the circuit and write equation to show that full-wave rectification is performed. **(08 Marks)**

OR

8 a. With a neat circuit diagram, explain 3-bit R-2R DAC. **(08 Marks)**

b. Explain the working of linear ramp ADC. **(06 Marks)**

c. With a neat block diagram, explain the operation of successive approximation analog to digital converter. **(06 Marks)**

Module-5

9 a. With a neat diagram, explain internal architecture of 555 timer. **(06 Marks)**

b. Explain the operating principle of phase locked loop. **(06 Marks)**

c. Explain monostable multivibrator circuit realized using IC 555 timer. Draw the circuit waveforms. **(08 Marks)**

OR

10 a. Design a circuit using 555 timer to be used as frequency divider. **(08 Marks)**

b. Define the following terms related to PLL (Phase Locked Loop).
i) Lock range ii) Capture range iii) Pull in time iv) Tracking range. **(04 Marks)**

c. A PLL system with 105 kHz input has VCO with 100 kHz free running frequency and sensitivity of 3.3 kHz/V. Phase detector has sensitivity 0.68 V/rad and amplifier gain of 5. Calculate : i) Loop again ii) Phase difference iii) Static error voltage iv) Tracking range. **(08 Marks)**

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