

Third Semester B.E. Degree Examination, Dec.2024/Jan.2025

Digital System Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With the help of block diagram, explain the general logic design sequence. (06 Marks)
- b. Place the following Boolean equations in to respective canonical forms
 i) $f(abc) = \bar{a}\bar{b} + ac + \bar{b}c$ ii) $f(pqr) = (p + \bar{q})(\bar{q} + r)$ (06 Marks)
- c. Find the minimal sum for the function using K-map $f(abcd) = \sum m(1, 2, 6, 7, 9, 11, 12, 15)$. (08 Marks)

OR

- 2 a. Design a digital circuit for implementing majority of four digital inputs. (07 Marks)
- b. Simplify the given Boolean expression using K-map
 $f(abcd) = \prod m(1, 2, 3, 4, 9, 10) + \prod d(0, 14, 15)$ (05 Marks)
- c. Find the prime implicants of the function using Quine-Muclusley method.
 $f(abcd) = \sum m(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$. (08 Marks)

Module-2

- 3 a. Design the full subtractor circuit using universal gates. (10 Marks)
- b. Design 4:16 decoder using two 3:8 decoder. (10 Marks)

OR

- 4 a. Explain the structure of Programmable Logic Array (PLA) with example. (06 Marks)
- b. Implement $f(pqrs) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$ using 4:1 MUX with p,q as select lines. (08 Marks)
- c. Implement the following POS function $f(pqr) = \prod (0, 1, 3, 5)$ using 3:8 decoder with active-high outputs. (06 Marks)

Module-3

- 5 a. What is race around condition? How can it be overcome by MS-JK flip-flop? (08 Marks)
- b. Define register and explain four bit SISO, SIPO, PISO, PIPO registers. (12 Marks)

OR

- 6 a. Bring out differences between synchronous and a synchronous counters. (05 Marks)
- b. With the help of output waveforms, explain 3-bit asynchronous counter. (08 Marks)
- c. Explain the working of twisted ring counter with necessary logic diagram and waveforms. (07 Marks)

Module-4

- 7 a. Design synchronous MOD-7 counter to count from 0 to 6. (12 Marks)
- b. Sequential circuit has one input and one output. The state diagram of the same is shown in Fig Q7(b). Design sequential circuit using D-flip-flop.

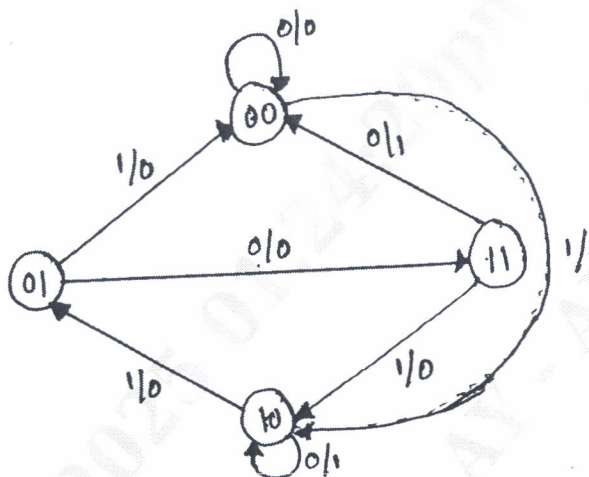


Fig Q7(b)

(08 Marks)

OR

- 8 a. Construct the transition table, state table, state diagram for Moore sequential circuit given in Fig Q8(a)

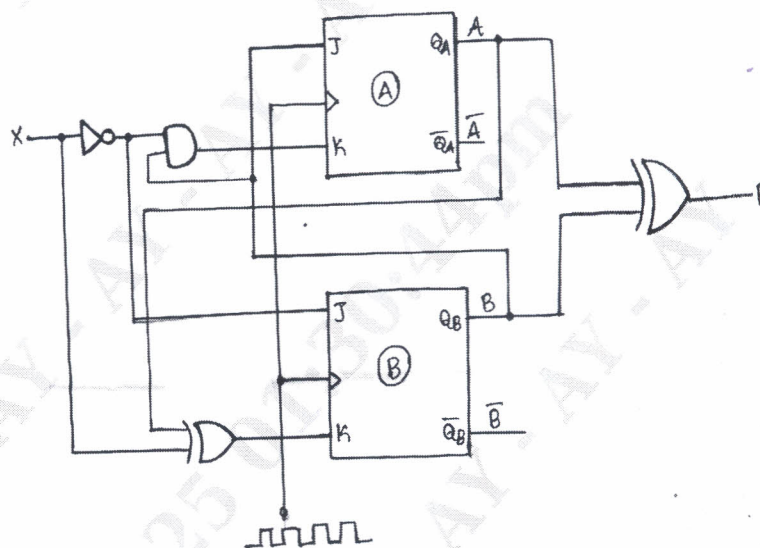


Fig Q8(a)

(10 Marks)

- b. Design a MOD – 6 synchronous counter using D-flipflop for the sequence 0 – 4 – 3 – 5 – 1 – 2

(10 Marks)

Module-5

- 9 a. Design a comparator using iterative circuits. (10 Marks)
b. With neat block diagram, explain serial adder with accumulator. (10 Marks)

OR

- 10 a. Design a binary divider circuits. (10 Marks)
b. List the guide line for constructions of state graphs. (10 Marks)
