

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025

Digital System Design using Verilog

Time: 3 hrs.

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.

2. M : Marks , L: Bloom's level , C: Course outcomes.

Module – 1				M	L	C
Q.1	a.	Design a combinational logic truth table so that an output is generated indicating when a majority of four inputs is true.		4	L3	CO1
	b.	Find the prime implicants and the essential prime implicants of the following Boolean functions using Karnaugh maps. i) $f(a, b, c, d) = \Sigma(1, 5, 6, 7, 11, 12, 13, 15)$ ii) $f(a, b, c, d) = \Sigma(0, 1, 4, 5, 9, 11, 13, 15)$		8	L4	CO1
	c.	Simplify the given boolean function using Quine McCluskey minimization technique for the function $O = f(a, b, c, d) = \Sigma(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$		8	L3	CO1
OR						
Q.2	a.	Place the following equations into the proper canonical form: i) $P = f(a, b, c) = ab' + ac' + bc$ ii) $G = f(w, x, y, z) = w'x + yz'$		4	L3	CO1
	b.	Find the minimal sum and minimal product for the following Boolean functions using Karnaugh maps i) $f(a, b, c, d) = \overline{a}b\overline{d} + bcd + a\overline{b}d + \overline{b}cd$ ii) $f(a, b, c, d) = (a + \overline{b})(a + c + d)(\overline{a} + \overline{b} + \overline{d})(a + \overline{c} + d)$		8	L4	CO1
	c.	Simplify the given boolean function using quine. McCluskey minimization technique for the function. $s = f(a, b, c, d) = \Sigma(1, 3, 13, 15) + \Sigma d(8, 9, 10, 11)$		8	L3	CO1
Module – 2						
Q.3	a.	Design and explain binary full adder with block diagram, Karnaugh map and logic circuit.		10	L3	CO2
	b.	Define decoder, write the symbol, truth table and logic circuit for 3:8 line decoder using minterm generator.		10	L2	CO2
OR						
Q.4	a.	Define multiplexer, write the symbol, truth table and logic circuit for 4:1 multiplexer using enable input.		10	L2	CO2
	b.	Realize the Boolean function $f(w, x, y, z) = \Sigma(0, 1, 5, 6, 7, 9, 12, 15)$ i) Using 8:1 MUX ii) Using 4:1 MUX		10	L2	CO2

Module – 3

Q.5	a.	Develop the characteristic equation for i) SR flip flop ii) JK flip flop iii) D flip flop iv) T flip flop.	10	L3	CO3
	b.	Explain serial in, parallel at unidirectional shift register and parallel in serious out unidirectional shift register.	10	L2	CO3

OR

Q.6	a.	Explain Mod-4 ring counter and Mod-8 twisted ring counter with logic diagram and counting sequence.	10	L2	CO3
	b.	Design a synchronous Mod-6 counter using clocked D-flip flop.	10	L3	CO3

Module – 4

Q.7	a.	Explain logical operators and relational operators used in verilog.	8	L2	CO4
	b.	Illustrate i) NETS ii) Register iii) Vector iv) integer data types with an example.	8	L2	CO4
	c.	Write a verilog code for full adder using data flow description style.	4	L2	CO4

OR

Q.8	a.	Illustrate the structure of behavioural description with an example using half adder.	8	L2	CO4
	b.	Illustrate the structure of verilog module with an example using half subtractor.	8	L2	CO4
	c.	Write a verilog code for binary to gray using behavioural description style.	4	L2	CO4

Module – 5

Q.9	a.	Write the syntax of IF and EISE-IF with an example.	8	L2	CO4
	b.	Write logic symbol, flowchart and program for D-latch using behavioural description style.	8	L2	CO4
	c.	Write a verilog code for 8:1 MUX using behavioural description style.	4	L2	CO4

OR

Q.10	a.	Explain the structure of structural model with built in gates using example of half adder. Also mention an primitive built in gates.	8	L2	CO4
	b.	Write a verilog code of a 3-bit ripple carry adder using structural description model.	8	L2	CO4
	c.	Write a verilog code of SR flip flop using behavioural description style.	4	L2	CO4
