CBCS SCHEME

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18EC42

Fourth Semester B.E. Degree Examination, Dec.2024/Jan.2025
Analog Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive the expression for Emitter current of a voltage divider bias and also discuss how to make I_E insensitive to variation in β and temperature. **(10 Marks)**

b. Design a collector to Base feedback resistor bias to obtain a dc current of 1 mA and to ensure ± 2V signal swing at the collector with $V_{CE} = 2.3$V. Assume $V_{CC} = 10$ V and $\beta = 100$. **(07 Marks)**

c What is trans-conductance of BJT and mention its significance? **(03 Marks)**

OR

2 a. Obtain the following expression of a BJT of small signal analysis.
i) Total instantaneous collector current
ii) Input resistance at the base **(10 Marks)**

b. Discus the following biasing scheme used in MOS
i) By fixing V_{GS}
ii) By fixing V_{GS} and connecting a resistance in the source. **(10 Marks)**

Module-2

3 a. Discuss the basic configuration of MOSFET. **(06 Marks)**

b. For a common source amplifier shown in Fig Q3(b), determine R_{in}, AV_0, R_0 and G_V

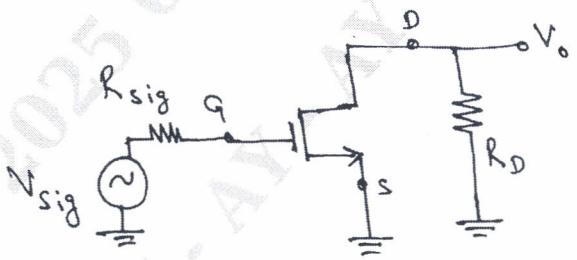

Fig Q3(b) **(14 Marks)**

OR

4 a. For an n-channel MOSFET with $t_{ox} = 10$nm, L = 1.0 µm, W = 10 µm, $L_{0V} = 0.05$ µm, $C_{sbo} = C_{dbo} = 10$ fF, $V_0 = 0.6$ V, $V_{SB} = 1$ V and $V_{DS} = 2$ V. Calculate C_{ox}, C_{ov}, C_{gs}, C_{gd}, C_{sb} and C_{db}. **(10 Marks)**

b. Explain the working of FET based phase shift oscillator and also mention the necessary conditions for sustained oscillation. **(10 Marks)**

Module-3

5 a. Explain the following properties of Negative. Feedback.
i) Gain, De-sensitivity ii) Bandwidth Extension iii) Noise reduction **(14 Marks)**

b. A negative feedback amplifier has a $A_f = 100$ and $A = 10^5$. What is the feedback factor? If a manufacturing error results in a reduction of A to 10^3, what is the closed loop voltage Gain? What is the percentage change in A_f? **(06 Marks)**

OR

6 a. Explain the working of class B output stage. **(08 Marks)**

b. For emitter follower Class A output stage $V_{cc} = 10V$, $I = 100$ mA and $R_L = 100\ \Omega$. If the output voltage is an 8 V – peak sinusoid, find :
i) Power delivered to load
ii) Average power drawn from the supplies
iii) Power conversion efficiency ignore the loss on Q_3 and R. **(06 Marks)**

c. Explain how cross over distortion can be eliminated to class AB output stage. **(06 Marks)**

Module-4

7 a. For the voltage Seri feedback amplifier, derive the expressions of
i) Exact voltage Gain ii) Input resistance with feedback iii) Output resistance with feedback **(14 Marks)**

b. For the inverting amplifier $R_1 = 470\ \Omega$ and $R_F = 4.7\ K\Omega$. Assume $A = 200000$, $R_i = 2\ M\Omega$, $R_o = 75\ \Omega$ and $f_o = 5$ Hz. Calculate A_F, R_{iF}, R_{OF} and f_F. **(06 Marks)**

OR

8 a. Explain the working of instrumentation amplifier using Transducer bridge with necessary equations. **(08 Marks)**

b. Explain the working of Inverting Schmitt trigger with input and output waveforms. **(08 Marks)**

c. For a Differential configuration summer $R = 1\ K\Omega$, $V_a = 2V$, $V_b = 3V$, $V_c = 4V$, $V_d = 5V$ and supply voltage of ± 15V. Determine the output voltage V_o. **(04 Marks)**

Module-5

9 a. Derive the expression of output voltage of a 4-bit Binary weighted resistor type DAC. Mention its disadvantages. **(10 Marks)**

b. Draw the block diagram of successive approximation ADC and explain it. **(10 Marks)**

OR

10 a. Explain the working of First order active Lowpass filter with the help of magnitude voltage gain and also design to get a cutoff frequency of 1 KHz with a passband gain of 2. **(10 Marks)**

b. Explain the working of Astable multi-vibration using 555 Timer and also derive the expression of Frequency of oscillation. **(10 Marks)**

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