CBCS SCHEME

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21EC52

Fifth Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Computer Organization and ARM Microcontrollers

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the pipelining and superscalar operation. **(05 Marks)**

b. Briefly explain the different key parameters that affects the processor performance. **(05 Marks)**

c. With a neat diagram, explain basic operational concept of computer. **(10 Marks)**

OR

2 a. Mention the difference between Big-endian and Little-endian assignments. **(05 Marks)**

b. Explain the different types of addressing modes. **(10 Marks)**

c. With diagram explain the Interrupt Hardware. **(05 Marks)**

Module-2

3 a. With diagram explain the internal organization of a 2M×8 dynamic memory chip. **(10 Marks)**

b. Explain the operations of synchronous DRAM. **(10 Marks)**

OR

4 a. Explain the different types of memories. **(10 Marks)**

b. With neat diagram explain the multiple bus organization. **(10 Marks)**

Module-3

5 a. Explain the architecture of ARM core dataflow model. **(10 Marks)**

b. With neat diagram explain the ARM based embedded system. **(10 Marks)**

OR

6 a. Explain the ARM condition flag register. **(05 Marks)**

b. What is pipeline? Explain the 3-stage ARM pipeline. **(05 Marks)**

c. Explain the architecture of ARM processor. **(10 Marks)**

Module-4

7 a. With example explain the following instructions:
i) ADC ii) EOR iii) SWI iv) UMULL v) SBC **(10 Marks)**

b. With neat diagram explain the ARM stack operation. **(10 Marks)**

OR

8 a. Explain the ARM Registers and also explain each. **(10 Marks)**

b. Explain the following ARMVSE extension instructions:
i) CLZ ii) QADD iii) QSUB iv) SMLAxy v) QDADD **(10 Marks)**

Module-5

9 a. Explain the following THUMB instructions:
i) TST ii) ROR iii) BX iv) BKPT v) ASR **(10 Marks)**

b. Discuss the ARM support basic C data types. **(10 Marks)**

OR

10 a. Explain the ARM function calls and loop operations. **(10 Marks)**

b. With example explain the single register and multiple register load store ARM instructions. **(10 Marks)**

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