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CBCS SCHEME

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18EC644

Sixth Semester B.E. Degree Examination, Dec.2024/Jan.2025
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain design methodology followed in IC industry with neat sketch. **(10 Marks)**

b. Develop a verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit. **(05 Marks)**

c. Develop a verilog model of a debouncer for a push-button switch that uses a debounder interval of 10 ms. Assume the system clock frequency is 50 MHz. **(05 Marks)**

OR

2 a. Explain the following constraints imposed in real world circuits:
(i) Noise margin (ii) Static levels (iii) Propagation delay
(iv) Static and dynamic power consumption. **(08 Marks)**

b. Develop a verilog model of a 4-to-1 multiplexer that selects among four unsigned 6-bit integers. **(04 Marks)**

c. Develop a datapath to perform a complex multiplication of two complex numbers. The operands and product are all in Cartesian form. The real and imaginary parts of the operands are represented as signed fixed point numbers with 4 pre-binary point and 12 post-binary-point bits. The real and imaginary parts of the product are similarly represented, but with 8-pre-binary point and 24 post-binary point bits. Area is the main constraint. **(08 Marks)**

Module-2

3 a. Determine whether there is an error in the ECC word 000111000100, and if so, correct it. **(05 Marks)**

b. Develop and explain a verilog model of a dual port 4K×16 - bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(05 Marks)**

c. Develop a 64K×8 - bit composite memory using four 16K×8 - bit components and also explain how memory components with tristate data outputs simplify the construction of larger memories. **(10 Marks)**

OR

4 a. What is the difference between asynchronous static RAM and synchronous static RAM? **(06 Marks)**

b. Design a FIFO to store upto 256 data items of 16 bits each, using a 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs, to indicate when the FIFO is empty and full. Assume that the FIFO will not be read when it is empty, not be written to when it is full, and that the write and read ports share a common clock. **(08 Marks)**

c. Write a symbol for basic memory component and explain its parts. **(06 Marks)**

Module-3

5 a. Explain with a neat diagram of the internal organization of a CPLD. **(06 Marks)**

b. Explain briefly bout the sequence of steps involved in IC manufacture. **(08 Marks)**

c. Distinguish between a platform FPGA from a simple FPGA? **(06 Marks)**

OR

6 a. Design 4-digit decimal counter with seven segment LED display with neat sketch using two 74LS390 dual decade counter, four 74LS47 BCD to seven segment decoder, four 7-segment display, plus any additional gates required. **(10 Marks)**

b. Explain different types of PCB design. **(05 Marks)**

c. Explain the differential signaling. **(05 Marks)**

Module-4

7 a. Explain any four serial interface standards. **(08 Marks)**

b. Show how 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(07 Marks)**

c. Explain neatly the designing of R-string DAC. **(05 Marks)**

OR

8 a. Design an develop the verilog code for an input controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. **(08 Marks)**

b. Explain the analog inputs used in input devices. **(04 Marks)**

c. Explain the concept of multiplexed buses. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(10 Marks)**

b. Explain the design optimization that are must to meet the design constraints. **(10 Marks)**

OR

10 a. Explain 4-bit LFST and CFSR for generating pseudorandom test vectors. **(10 Marks)**

b. Explain logical partitioning and physical partitioning of a transport monitoring system. **(10 Marks)**

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