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18EC72

Seventh Semester B.E. Degree Examination, Dec.2024/Jan.2025
VLSI Design

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With relevant diagrams, explain the operation of nmos enhancement mode transistor for 3 different regions of operation. **(08 Marks)**

   b. Explain the operation of mux based positive edge triggered D-flip flop with neat circuit and waveform. **(08 Marks)**

   c. Explain the operation of tri-state inverter. **(04 Marks)**

OR

2 a. Explain the following non-ideal I-V effects :
       i) Velocity saturation and mobility degradation
       ii) Channel length modulation **(08 Marks)**

   b. Discuss the DC characteristics of CMOS inverter with necessary tabulation. **(08 Marks)**

   c. Write a short note on noise margin. **(04 Marks)**

Module-2

3 a. Draw and explain the cross sections while manufacturing n-well. **(08 Marks)**

   b. Define the following with respect to MOS fabrication process:
       i)   Photo lithography
       ii) Oxidation
       iii) Chemical vapor deposition
       iv) Self aligned process. **(06 Marks)**

   c. Draw the circuit and standard cell layout of 3 - i/p NAND gate **(06 Marks)**

OR

4 a. What is scaling? Why scaling is needed? Assume that scaling factor s = 1.24 and current process technology is 180 nm. What is the gate length of the new technology? **(04 Marks)**

   b. Explain constant field scaling? What is the effect of constant field scaling on C_{ox} , I_D , power dissipation and power density. **(08 Marks)**

   c. Explain the following limitations imposed by small-device geometries:
       i) DIBL   ii) Drain punch through **(08 Marks)**

Module-3

5 a. Define the following timing parameters:
   i) Propagation delay time   ii) Contamination delay time
   iii) Rise time   iv) Fall time   **(04 Marks)**

   b. Explain Elmore delay. Compute the Elmore delay for V_{out} in the below given second order RC system. [Refer Fig.Q5(b)]

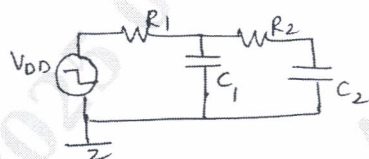Fig.Q5(b)   **(06 Marks)**

   c. What is logical effort? Discuss and calculate the logical effort for inverter, 3- i/p NAND gate and 3 i/p NOR gate.   **(10 Marks)**

OR

6 a. Explain cascode voltage switch logic circuits with an example of 2 i/p AND/NAND logic gate. Mention any 2 advantages and limitations.   **(08 Marks)**

   b. What is ratioed circuits? Explain pseudo nMOS and ganged CMOS logic circuits. **(08 Marks)**

   c. Write a short note on complementary pass transistor logic (CPL).   **(04 Marks)**

Module-4

7 a. Discuss various conventional CMOS latches.   **(10 Marks)**

   b. Explain pulsed latch with relevant waveform.   **(06 Marks)**

   c. What is synchronous resettable latch?   **(04 Marks)**

OR

8 a. Explain the operation of dynamic D-latch and discuss charge leakage when clock goes to zero.   **(08 Marks)**

   b. Explain the operation of ratioless logic enhancement - load dynamic shift register. **(05 Marks)**

   c. Explain the working of dynamic CMOS logic circuit with an example. Also discuss its limitations.   **(07 Marks)**

Module-5

9 a. Explain the operation of 3-Transistor DRAM cell with read/write circuitry and typical waveforms.   **(10 Marks)**

   b. Explain the Read and Write operation in 6T-SRAM cell with read and write timing diagram. **(10 Marks)**

OR

10   Write a short note on :
   a. Testers and test fixtures

   b. Observability and controllability

   c. Adhoc testing

   d. Built-In Self Test (BIST)   **(20 Marks)**