CBCS SCHEME

USN | | | | | | | | | | |

21EC71

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Advanced VLSI

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain ASIC design flow with neat flow chart. **(10 Marks)**

b. Explain Booth Encoding multiplier with an example. **(10 Marks)**

OR

2 a. Describe different cell compilers and I/O cells. **(10 Marks)**

b. With a neat diagram, explain the operation of conditional sum adder. Mention its advantages and disadvantages. **(10 Marks)**

Module-2

3 a. Explain the concept of measurement of delay in Floorplanning. **(10 Marks)**

b. Explain the following :

i) Power planning ii) Clock planning **(10 Marks)**

OR

4 a. Write an algorithm for iterative placement improvement method and explain briefly. **(10 Marks)**

c. Explain the goals and objectives of global routing in detail. **(10 Marks)**

Module-3

5 a. Explain factors in randomizing the stimulus to a design. **(10 Marks)**

b. Draw the diagram of layered test bench of system verilog and describe the function of each layer. **(10 Marks)**

OR

6 a. Describe the various array methods with an example. **(08 Marks)**

b. Describe type def and enumerated data types with example. **(06 Marks)**

c. Explain constant and strings in system verilog with example. **(06 Marks)**

Module-4

7 a. Explain Tasks, functions and void function in system verilog. **(06 Marks)**

b. How time values are specified in system verilog, describe with example. **(06 Marks)**

c. Explain automatic storage and variable initialization with system verilog program example. **(08 Marks)**

OR

8 a. Describe the communication between the test bench and DUT with suitable diagram and system verilog program. **(10 Marks)**

b. Explain different types of system verilog assertions with example. **(10 Marks)**