CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, June/July 2025
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the working principle of opto couples with neat diagram. **(06 Marks)**

b. Derive an expression for collector current and collector emitter voltage of fixed bias circuit. **(06 Marks)**

c. For the circuit shown in the Fig Q1(c). Draw DC load line, use silicon transistor with B = 50 and V_{BE} = 0.7V

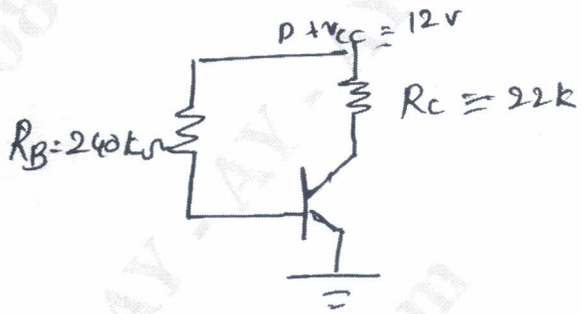

Fig Q1(c) **(08 Marks)**

OR

2 a. With the help of a neat circuit diagram and wave form explain the working principle of Relaxation oscillator. **(10 Marks)**

b. Explain current to voltage converter. **(05 Marks)**

c. Define voltage Regulator. Explain adjustable voltage regulator. **(05 Marks)**

Module-2

3 a. Simply the following function using K-map and obtain simplified Boolean expressions.
i) $f_1(a, b, c, d) = \Sigma m (1, 3, 4, 5, 7, 10, 12)$
ii) $f_2(a, b, c, d) = \Sigma m (5, 8, 9, 10, 11, 12, 13, 14, 15)$ **(10 Marks)**

b. Find all the prime implicants of function using Q-M method.
$f(a, b, c, d) = \Sigma m (0, 2, 3, 4, 8, 10, 12, 13, 14)$. **(10 Marks)**

OR

4 a. For the following function use Q-M method and obtain simplified expression.
$f(a, b, c, d) = \Sigma m (7, 9, 12, 13, 14, 15) + dc(4, 11)$ **(08 Marks)**

b. With an example, explain Petrik's method. **(06 Marks)**

c. For the given function determine minimal sum using MEV technique. Use 'd' as MEV variable
$f(a, b, c, d) = \Sigma m(3, 4, 5, 7, 8, 11, 12, 13, 15)$. **(06 Marks)**

Module-3

5 a. Define static – 1 hazard. Explain how static – 1 hazard can be detected and removed with an example. **(08 Marks)**

b. What is multiplexer and explain 8 to 1 MUX with the help of logic diagram and corresponding expression. **(06 Marks)**

c. Explain the importance of 3-state Buffer. **(06 Marks)**

OR

6 a. Implement the following functions using 3 : 8 Decodes.
$f_1(a, b, c) = \Sigma m(0, 4, 6, 7)$
$f_2(a, b, c) = \Sigma m(1, 4, 5)$. **(06 Marks)**

b. Implement the following Boolean function using an appropriate PLA
$f_1(a, b, c) = \Sigma m(0, 4, 7)$
$f_2(a, b, c) = \Sigma m(4, 6,)$ **(06 Marks)**

c. Realize a full adder using PAL. **(08 Marks)**

Module-4

7 a. Explain the structure of HVDL program, write VHDL code for 4-bit parallel adder using full adder as component. **(08 Marks)**

b. With necessary diagrams, explain switch debouncing with SR latch. **(06 Marks)**

c. Explain D Flip-Flop with the help of timing diagram. **(06 Marks)**

OR

8 a. Give the implementation of T-Flip-flop from D-Flip-Flop. **(04 Marks)**

b. Explain Master – Slave JK-Flip-Flop operation. **(08 Marks)**

c. Derive the characteristics equation of following flip-flops
i) SR Flip-Flop ii) D Flip-Flop iii) T Flip-Flop iv) JK Flip-Flop. **(08 Marks)**

Module-5

9 a. With a neat sketch, explain the working principle of Serial In and Serial Out (SISO) shift Register. **(06 Marks)**

b. Design 3 bit synchronous Binary counter using Transition table of T-flip-flop. **(08 Marks)**

c. Explain how 4 bit Register with data, load, clear and clock input is constructed using D Flip-Flops. **(06 Marks)**

OR

10 a. With the help of state graph, state and transition diagram, explain sequential parity checker. **(10 Marks)**

b. With the help of neat block diagram, explain the working principle of n-bit parallel adder with accumulator. **(10 Marks)**

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