CBCS SCHEME

USN | | | | | | | | | | |

21CS34

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, analyze the basic operational concepts of a computer. Give the operating steps. **(06 Marks)**

b. Explain the basic instruction types with examples. **(04 Marks)**

c. Explain: (i) Processor clock
(ii) Clock rate
(iii) Basic performance equation
(iv) Performance measurement **(10 Marks)**

OR

2 a. Define addressing mode, explain any three addressing modes with examples. **(10 Marks)**

b. Write an assembly program that reads a line of characters and displays it. **(06 Marks)**

c. Explain Big-Endian and Little-Endian addressability. **(04 Marks)**

Module-2

3 a. Define Interrupt. Explain various ways of enabling and disabling interrupts. **(08 Marks)**

b. With a neat diagram, explain any three methods for handling multiple interrupt requests raised by multiple devices. **(12 Marks)**

OR

4 a. With a neat diagram, explain DMA. Briefly explain centralized bus arbitration technique. **(10 Marks)**

b. Explain synchronous and Asynchronous bus with timing diagrams. **(10 Marks)**

Module-3

5 a. With a neat diagram, explain the internal organization of 128×8 memory chip. **(10 Marks)**

b. What is cache memory? Explain the direct and associative mapping techniques. **(10 Marks)**

OR

6 a. What is memory interleaving? Explain with an example. **(10 Marks)**

b. Define Virtual memory. Explain the address translation. **(10 Marks)**

Module-4

7 a. Draw 4-bit carry-look-ahead adder and explain. **(10 Marks)**

b. Perform multiplication for +13 and −6 using Booth's algorithm. Explain Booth's algorithm. **(10 Marks)**

OR

8 a. Explain three-bus organization of data path with a neat diagram. **(06 Marks)**

b. Explain Hard wired control unit organization in a processing unit. **(06 Marks)**

c. Write actions required and control sequence for execution of instruction ADD (R3), R1. **(08 Marks)**

Module-5

9 a. Define Parallel Processing. Explain processor with multiple functional units. **(10 Marks)**
b. Define Pipelining. Explain five stage instruction pipeline with timing diagram. **(10 Marks)**

OR

10 a. Explain arithmetic pipeline with suitable example. **(10 Marks)**
b. Explain instruction pipeline with suitable example. **(10 Marks)**

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