CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Design a combinational logic circuit which takes two, 2-bit binary numbers as its input and generates an output equal to 1, when the sum of the two numbers is even.	6	L1	CO1
	b.	Develop the canonical forms for the following Boolean equations: i) $a + b(a + c) + bc$ ii) $(a + b)(c + d)$	6	L1	CO1
	c.	Find all the prime implicants and essential prime implicants for the following functions using k-map method: i) $P = f(a, b, c, d) = \sum(1, 2, 3, 5, 6, 7, 11, 12, 13, 14, 15)$ ii) $S = f(a, b, c, d) = \prod(0, 2, 3, 8, 9, 10, 12, 14)$	8	L2	CO1
		OR			
Q.2	a.	Simplify the following Boolean functions using k-map. Draw the logic diagram for the simplified equation: i) $w = f(a,b,c,d) = \sum(1,5,7,9,13,15) + \sum d(8,10,11,14)$ ii) $y = f(a,b,c,d) = \pi(0,2,3,4,5,12,13) + \pi d(8,10)$	10	L2	CO1
	b.	Solve the following Boolean function by using Quine-McClusky method. Verify using k-map $s = f(w,x,y,z) = \sum(2,3,4,5,13,15) + \sum d(8,9,10,11)$	10	L2	CO1
		Module – 2			
Q.3	a.	Realize the following functions using 3:8 decoder along with OR and/or NOR gates. In each case the gates should be selected so as to minimize their total number of inputs. i) $f_1(a,b,c) = \sum m(1,3,6)$ and $f_2(a,b,c) = \sum m(2,5,7)$ ii) $f_1(a,b,c) = \Pi M(0,3,5,6,7)$ and $f_2(a,b,c) = \Pi M(2,3,4,5,7)$	7	L2	CO2
	b.	Design a priority encoder for a system with three inputs, the middle bit with highest priority encoded as 10, MSB with next priority encoded as 11 and LSB with least priority encoded as 01. Write functional table and its logic diagram.	5	L2	CO2
	c.	Explain carry look ahead adder with sigma block and necessary equations.	8	L2	CO2

		OR			
Q.4	**a.**	Implement the function $S = f(a,b,c,d) = \sum(1,3,4,11,12,13,14,15)$ using i) 8:1 MUX and ii) 16:1 MUX	**7**	**L2**	**CO2**
	b.	Design a single decade decimal adder with necessary correction circuit.	**8**	**L2**	**CO2**
	c.	Explain briefly Programmable Array Logic (PAL).	**5**	**L2**	**CO2**
		Module – 3			
Q.5	**a.**	Construct the logic diagram of master slave JK flipflop and its truth table. Explain with necessary timing diagram.	**8**	**L2**	**CO3**
	b.	Construct Johnson counter using positive edge triggered flipflops and explain with necessary truth table.	**8**	**L2**	**CO3**
	c.	Derive the characteristic equation of SR flipflop.	**4**	**L2**	**CO3**
		OR			
Q.6	**a.**	Explain universal shift register with the help of logic diagram and mode control table.	**10**	**L2**	**CO3**
	b.	Design a mod-6 synchronous counter with the sequence 0 – 2 – 5 – 6 – 4 – 3 using T flipflops.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Explain the following data types in verilog with example: i) Nets ii) Registers iii) Integer iv) Parameter	**8**	**L2**	**CO4**
	b.	Evaluate the following if A = 0011, B = 0100, E = 4 and F = 2 i) A * B ii) A + B iii) E * * F iv) A & B v) A < < 2 vi) {A[3], B}	**6**	**L2**	**CO4**
	c.	Write a verilog data flow model for full subtractor.	**6**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain three styles of description available in verilog with half adder example.	**9**	**L2**	**CO4**
	b.	Realize 2 × 1 multiplexer with active low enable and also write the Verilog program by considering delay time to signal assignment statements. Also draw simulation waveform.	**7**	**L2**	**CO4**
	c.	Write a short note on signal assignment in verilog with an example.	**4**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Explain the following sequential statements in verilog : i) For loop ii) While loop iii) Repeat iv) Forever.	**8**	**L1**	**CO4**
	b.	Write a verilog behavioral description for JK flipflop along with the design and timing diagram.	**8**	**L2**	**CO4**

	c.	Explain different case statements in verilog.	4	L2	CO4
		OR			
Q.10	a.	Write a verilog program for 3-bit ripple carry adder using structural description.	8	L2	CO4
	b.	Realize the binary up-down counter using verilog behavioral description.	7	L3	CO4
	c.	Explain if-else-if statement in verilog with an example.	5	L2	CO4

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