CBCS SCHEME

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18MT36



# Third Semester B.E. Degree Examination, June/July 2025
## Computer Organization & Architecture

Time: 3 hrs. Max. Marks: 100

**Note:** ***Answer any FIVE full questions, choosing ONE full question from each module.***



### Module-1

1 a. Describe interconnection between memory and processor with a neat diagram. **(05 Marks)**

b. Perform the following arithmetic operation using 2's complement representation. Assume 4 bit representation where applicable i) 5 – 2 ii) –2 – 3 iii) 7 + 3 iv) –6 + 5. **(10 Marks)**

c. Explain Big Endian and Little Endian memory representation. **(05 Marks)**

**OR**

2 a. Describe basic functional unit of a computer with a neat diagram. **(05 Marks)**

b. Illustrate working of branch instruction with a help of an example that adds first n natural numbers. **(10 Marks)**

c. Explain the following : i) Basic performance equation ii) Processor clock. **(05 Marks)**

### Module-2

3 a. Discuss any five commonly used assembler directives in assembly language programming along with their purpose. **(10 Marks)**

b. Demonstrate parameter passing through registers using an assembly language program. **(10 Marks)**

**OR**

4 a. Discuss the following addressing nodes with an example :
i) Indirect addressing ii) Indexed addressing. **(10 Marks)**

b. Demonstrate the working of logical and arithmetic instructions with suitable example. **(10 Marks)**

### Module-3

5 a. Explain the mechanism of enabling and disabling interrupts at the processor and I/O device levels. **(10 Marks)**

b. Discuss the methods used by processor to control and manage I/O device request including polling and interrupt driven approaches. **(10 Marks)**

**OR**

6 a. Explain how multiple interrupt requests are handled by processor and explain the significance of interrupt nesting and interrupt vectors in this context. **(10 Marks)**

b. Explain the priority schemes used by a processor to manage simultaneous I/O interrupt request from multiple devices. **(10 Marks)**

## Module-4

7 a. With the help of a diagram, explain the internal organization of static RAM cell. **(10 Marks)**

b. Explain the internal organization of 2m × 8 DRAM chip with a neat diagram. **(10 Marks)**

**OR**

8 a. Explain the structure and operation of virtual memory with a neat diagram. **(10 Marks)**

b. Discuss the various cache mapping techniques with appropriate diagram. **(10 Marks)**

## Module-5

9 a. Describe three – bus organization of datapath with a neat diagram. **(10 Marks)**

b. Explain micro-programmed control unit organization with a neat diagram. **(10 Marks)**

**OR**

10 a. Describe hardwired control unit-organization with a neat diagram. **(10 Marks)**

b. Discuss the complete control sequence for the execution of instruction Add $(R_2)$ $R_1$. **(10 Marks)**

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