CBCS SCHEME

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BMT304

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

			M	L	C
		Module – 1			
Q.1	a.	Describe with a neat diagram connection between processor and computer memory.	10	L2	CO1
	b.	Explain Big-endian and little-endian method with neat diagram.	10	L2	CO1
		OR			
Q.2	a.	What is straight line sequencing? Explain with example program.	10	L2	CO1
	b.	Write the basic performance equation. Explain the role of each of the parameter in the equation.	10	L2	CO1
		Module – 2			
Q.3	a.	Explain following addressing modes with examples : (i) Direct mode (ii) Immediate mode (iii) Indexed mode	10	L2	CO1
	b.	Register R_1 and R_2 of a computer contains the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions: i) Load $20(R_1)$, R_5 ii) Move #3000, R_5 iii) Add $-(R_2)$, R_5	10	L3	CO1
		OR			
Q.4	a.	Develop an assembly language program that reads n numbers from memory, sums them and stores the result in a register.	10	L3	CO1
	b.	What is stack? Explain with example a routine for safe push operation and safe pop operation.	10	L2	CO1
		Module – 3			
Q.5	a.	Discuss the different schemes available to enable and disable interrupts.	10	L2	CO2
	b.	What is interrupt nesting? Explain with a neat diagram the implementation of interrupt priority using individual interrupt request and acknowledge lines.	10	L2	CO2
		OR			
Q.6	a.	What is DMA? With a neat diagram discuss how DMA controller register accessed by the processor to initiate transfer operations.	10	L2	CO2
	b.	Explain how simultaneous interrupt request from several I/O devices will be handled by a processor through a single INTR line.	10	L2	CO2

		Module – 4			
Q.7	**a.**	Discuss internal organization of 2M × 8 dynamic memory chips.	**10**	**L3**	**CO3**
	b.	Explain the memory hierarchy with neat diagram.	**10**	**L2**	**CO3**
		OR			
Q.8	**a.**	Draw the organization of 1K × 1 memory chip and explain its working.	**10**	**L3**	**CO3**
	b.	Define ROM. List and explain various types of ROMs.	**10**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Explain single bus organization of datapath with a neat block diagram.	**10**	**L2**	**CO4**
	b.	Explain the hardwired control unit organization in a processing unit.	**10**	**L2**	**CO4**
		OR			
Q.10	**a.**	Explain the microprogrammed control unit organization in a processing unit.	**10**	**L2**	**CO4**
	b.	Write the control sequence for instruction execution for Add (R_3), R_1 in the execution of a complete instruction.	**10**	**L2**	**CO4**

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